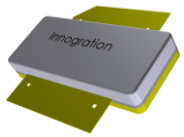
2500MHz-2700MHz, 150W, 28V High Power RF LDMOS FETs

Description

The ITCH27150C2 is a 150-watt, internally matched LDMOS FET, designed for multicarrier WCDMA/PCS/DCS/LTE base station and ISM applications with frequencies from 2500 to 2700 MHz. It Can be used in Class AB/B and Class C for all typical cellular base station modulation formats.

ITCH27150C2



•Typical Performance (On Innogration fixture with device soldered):

VDD = 28 Volts, I_{DQ} = 1000 mA, Pulse CW, Pulse Width=100 us, Duty cycle=10% .

Freq	P1dB	P1dB	P1dB Eff	P1dB Gain	P3dB	P3dB	P3dB Eff
(MHz)	(dBm)	(W)	%	dB	(dBm)	(W)	%
2500	51.70	148.10	51.20	13.35	52.55	179.90	52.10
2600	52.18	165.40	52.20	13.06	53.02	200.60	53.70
2700	51.78	150.80	51.90	12.55	52.56	180.20	53.50

ACPR @43dBm_1C-WCDMA			
Freq (MHz)	ACPR (dBc)	Gain (dB)	Efficiency (%)
2500	-40.80	14.90	20.00
2600	-42.90	14.50	19.10
2700	-41.30	14.00	19.30

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	70	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.3	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=1mA)	V_{DSS}	65	70		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}			10	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 uA)	$V_{GS(th)}$		1.8		V
Gate Quiescent Voltage (V_{DD} = 28 V, I_{DQ} = 1000 mA, Measured in Functional Test)	$V_{GS(Q)}$	2.3	2.8	3.3	V
Functional Tests (On Innogration demo, 50 ohm system) : V_{DD} = 28 Vdc, I_{DQ} = 1000 mA, f = 2700 MHz, Pulse CW, Pulse Width=20 us, Duty cycle=10% .					
Power Gain（Maximum Gain）	G_p		14.8		dB
1 dB Compression Point	P_{-1dB}		51.6		dBm
3dB Compression Point	P_{-3dB}		52.3		dBm
Drain Efficiency@P3dB	η_D		50.1		%
Input Return Loss	IRL		-7		dB

Load Mismatch (On Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 1000 mA, f = 2700 MHz

VSWR 10:1 at 150W pulse CW Output Power	No Device Degradation

Reference Circuit of Test Fixture Assembly Diagram

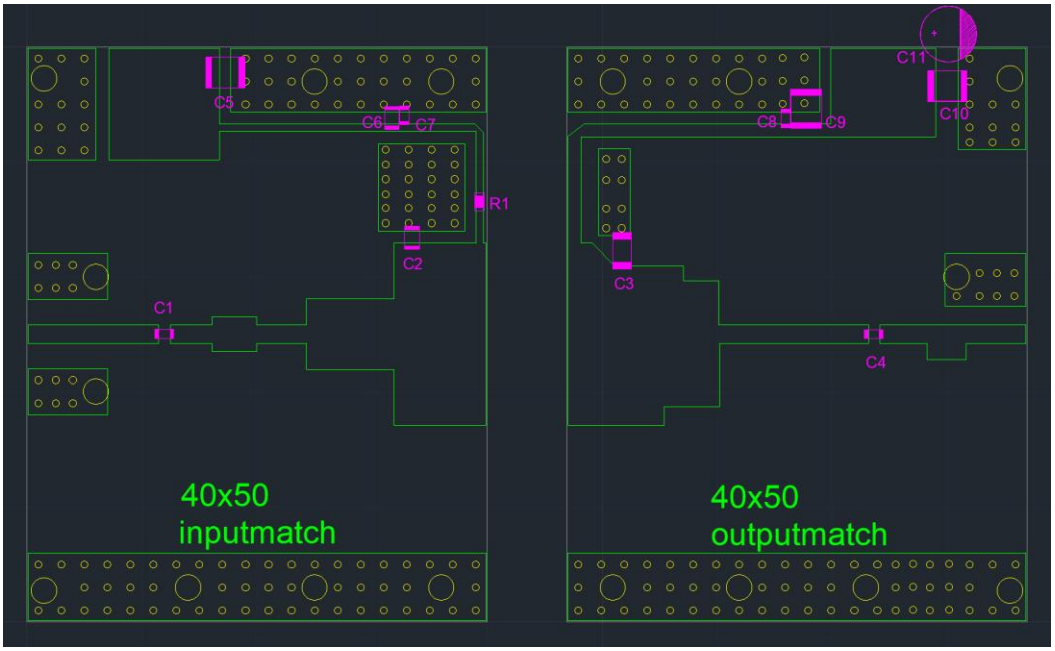


Figure 1. Test Circuit Component Layout

Table 1. Test Circuit Component Designations and Values

Reference	Footprint	Value	Quantity
C1	0603	3.3pF	1
C2	0805	0.8pF	1
C3	0805/1206	0.8pF	1
C4,C7,C8	0603	8.2pF	3
C6	0806	10uF	1
R1	0603	10ohm	1
C5,C9,C10	1210	10uF/63V	3
C11	\	470uF/63V	1
U1	C2	ITCH27150C2	1

TYPICAL CHARACTERISTICS

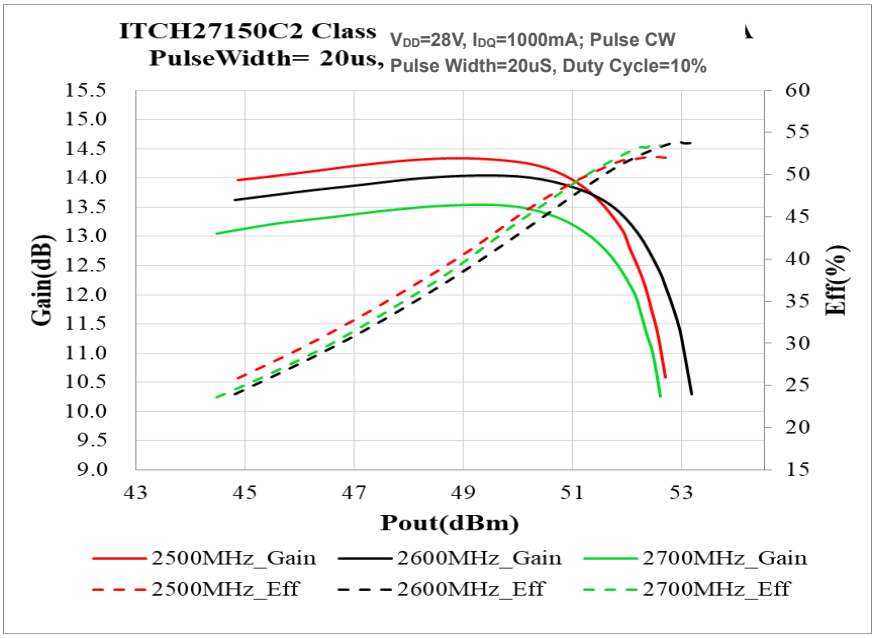


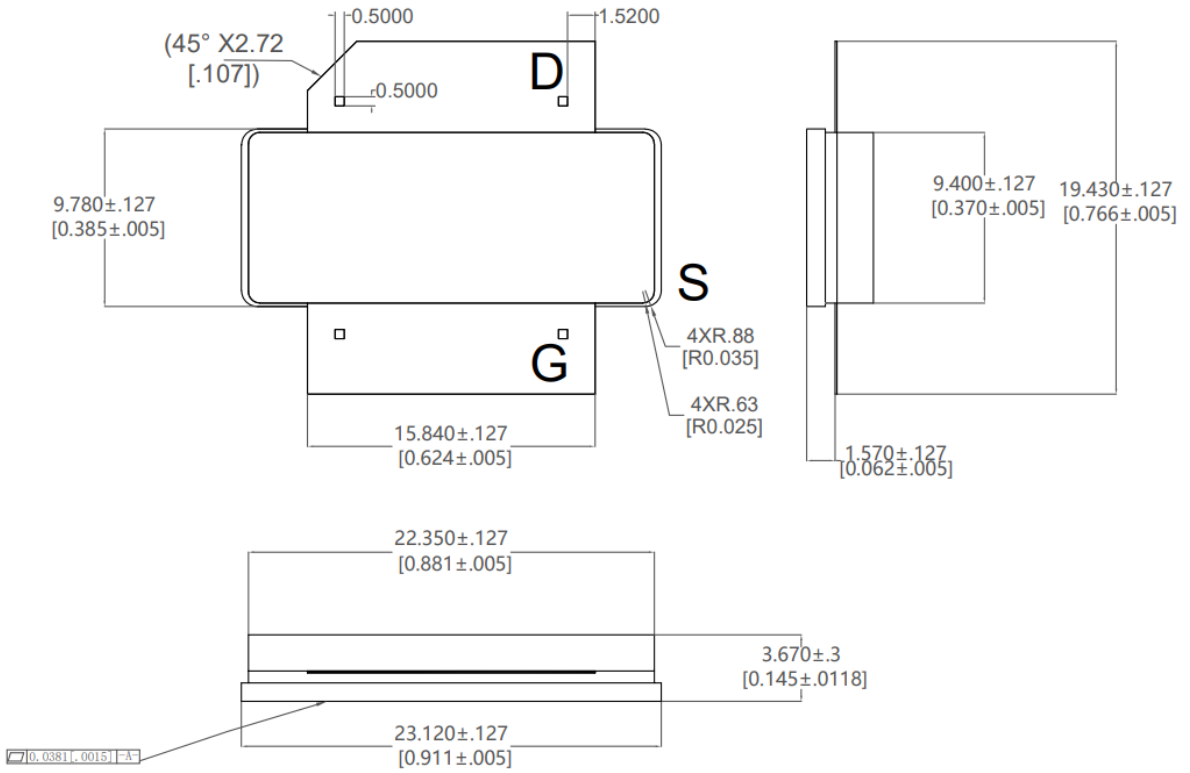
Figure 2. Power gain and drain efficiency as function of Pulse output power（2500MHz-2700MHz）

Figure 3. Network analyzer output S11/S21

Package Outline

Flangeless ceramic package;

INP-688-2-EL（C2)



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2018/12/04	Rev 1.0	Preliminary Datasheet
2024/7/24	Rev 2.0	Change application data according to new tuning

Application data based on CWZ-24-17

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