

MR1503 LDMOS TRANSISTOR

Document Number: MR1503
Preliminary Datasheet V1.0

25W, 28V High Power RF LDMOS FETs

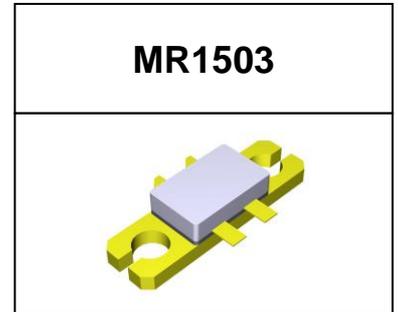
Description

The MR1503 is a 25-watt, unmatched, push pull LDMOS FETs, designed for Wide-band and Mobile radio applications with frequencies under 1500MHz. It can be used in Class AB/B and Class C for all typical modulation formats.

- Typical Performance (On Innogration fixture with device soldered):

$V_{DD} = 28$ Volts, $I_{DQ} = 200$ mA, CW.

Frequency	Gp (dB)	P _{-1dB} (W)	$\eta_D@P_{-1}$ (%)
1000 MHz	22	25	62



Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+40	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c = 85^\circ\text{C}$, $T_j = 200^\circ\text{C}$, DC test	$R_{\theta JC}$	1.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics (per half section)

Drain-Source Voltage $V_{GS}=0, I_{DS}=1.0mA$	$V_{(BR)DSS}$	90	95		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28 V, V_{GS} = 0 V$)	I_{DSS}	---	---	1	μA
Gate--Source Leakage Current ($V_{GS} = 9 V, V_{DS} = 0 V$)	I_{GSS}	---	---	1	μA
Gate Threshold Voltage ($V_{DS} = 28V, I_D = 600 \mu A$)	$V_{GS(th)}$	---	2.11	---	V
Common Source Input Capacitance ($V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz$)	C_{ISS}		16.2		pF
Common Source Output Capacitance ($V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz$)	C_{OSS}		5.9		pF
Common Source Feedback Capacitance ($V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz$)	C_{RSS}		0.5		pF

Functional Tests (On Demo Test Fixture, 50 ohm system) $V_{DD} = 28 Vdc, I_{DQ} = 200 mA, f = 1000 MHz, CW$ Signal Measurements.

Power Gain	G_p		22		dB
Drain Efficiency@P1dB	η_D		62		%
1 dB Compression Point	P_{-1dB}		25		W
Input Return Loss	IRL		-10		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 28 Vdc, I_{DQ} = 200 mA, f = 1000 MHz$

VSWR 10:1 at 20W pulse CW Output Power	No Device Degradation
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Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads

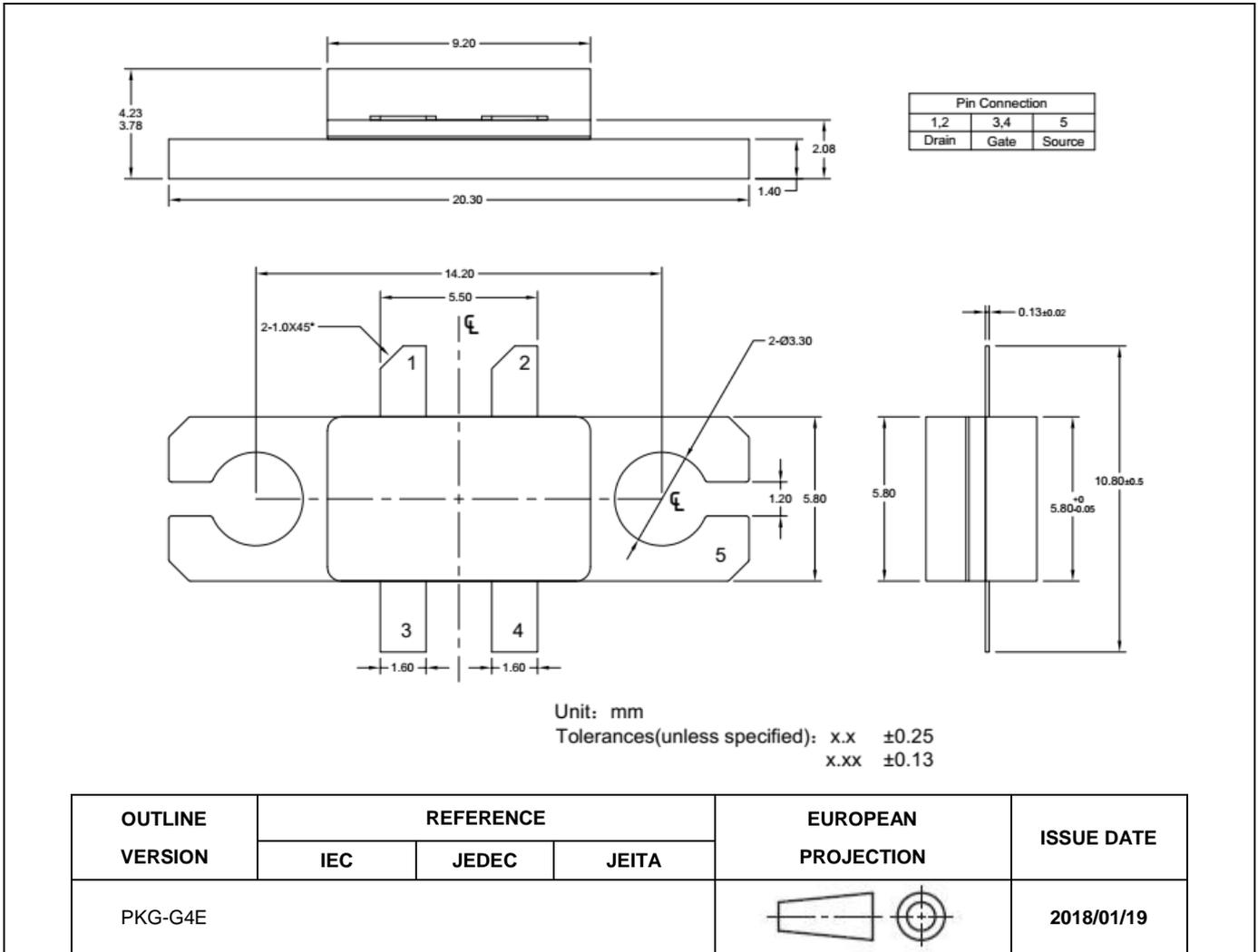


Figure 1. Package Outline PKG-G4E

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2018/8/15	Rev 1.0	Product datasheet creation

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