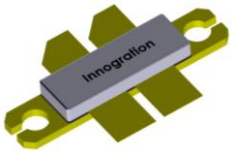
MX0535VPX LDMOS TRANSISTOR

Document Number: MX0535VPX
Preliminary Datasheet V1.1

350W, 50V High Power RF LDMOS FETs

MX0535VPX



Description

The MX0535VPX is a 350-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 0.5 GHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.

- Typical narrowband performance(on 325/500MHz test board with device soldered):
  V_{DD} = 50 Volts, I_{DQ} = 200 mA, CW.

Freq (MHz)	P3dB (W)	Gain (dB)	Eff (%)
325	380	16.2	67.3

- Typical broadband performance(on 400-460MHz test board with device soldered):

MX0535VPX GW VGS=3.28V VDS=48V IDQ=100mA CW

Freq (MHz)	Psat (dBm)	Psat (W)	IDS (A)	Pin (dBm)	Gain (dB)	Eff(%)	2nd （dBc）	3rd （dBc）
400	55.12	325.1	9.60	40.00	15.12	70.55	-21.20	-21.30
410	55.08	322.1	9.57	40.00	15.08	70.12	-21.50	-20.60
420	55.03	318.4	9.48	40.05	14.98	69.98	-21.50	-19.40
430	54.90	309.0	9.18	40.22	14.68	70.13	-20.80	-18.40
440	54.72	296.5	8.85	40.50	14.22	69.79	-20.90	-16.70
450	54.68	293.8	8.72	40.60	14.08	70.18	-21.80	-13.30
460	54.80	302.0	8.61	40.45	14.35	73.07	-23.20	-11.10

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+135	Vdc
Gate--Source Voltage	V_{GS}	-9 to +11	Vdc
Operating Voltage	V_{DD}	+55	Vdc

Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.25	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0Ma	$V_{(BR)DSS}$		135		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.65	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.35	——	V
Drain source on state resistance (Vds=0.1V, Vgs=10V)	Rds(on)		352		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{ISS}		141		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{OSS}		42		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{RSS}		0.7		pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 200 mA, f = 500MHz, pulse width:100us, duty cycle:10%

Load 10:1 All phase angles, at 350W Pulsed CW Output Power	No Device Degradation

325MHz
Reference Circuit of Test Fixture Assembly Diagram

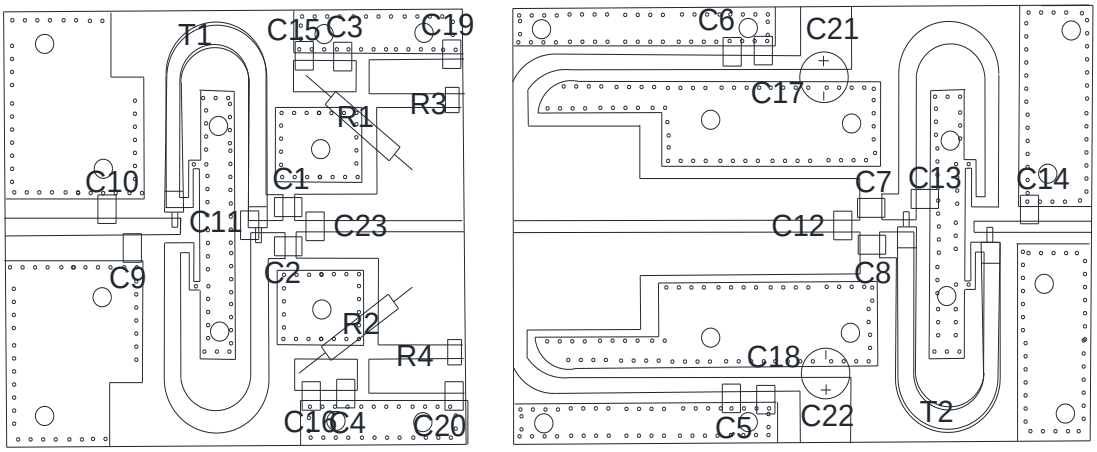


Figure 1. Test Circuit Component Layout (325M)

Table 1. Test Circuit Component Designations and Values (325M)

Part	description	Model
C1~C6	220PF	DLC70B
C13	3PF	DLC70B
C7, C8	100PF	ATC800B
C9	20PF	DLC70B
C10	1.5PF	DLC70B
C11	15PF	DLC70B
C12	12PF	DLC70B
C14	6.8PF	ATC800B
C15~c18	10UF	100V/10UF
C21, c22	470UF	63V/470UF
C23	18PF	DLC70B
R1	100Ω	
R2	16Ω	1206
T1,T2	55mm	SF-86-25

TYPICAL CHARACTERISTICS

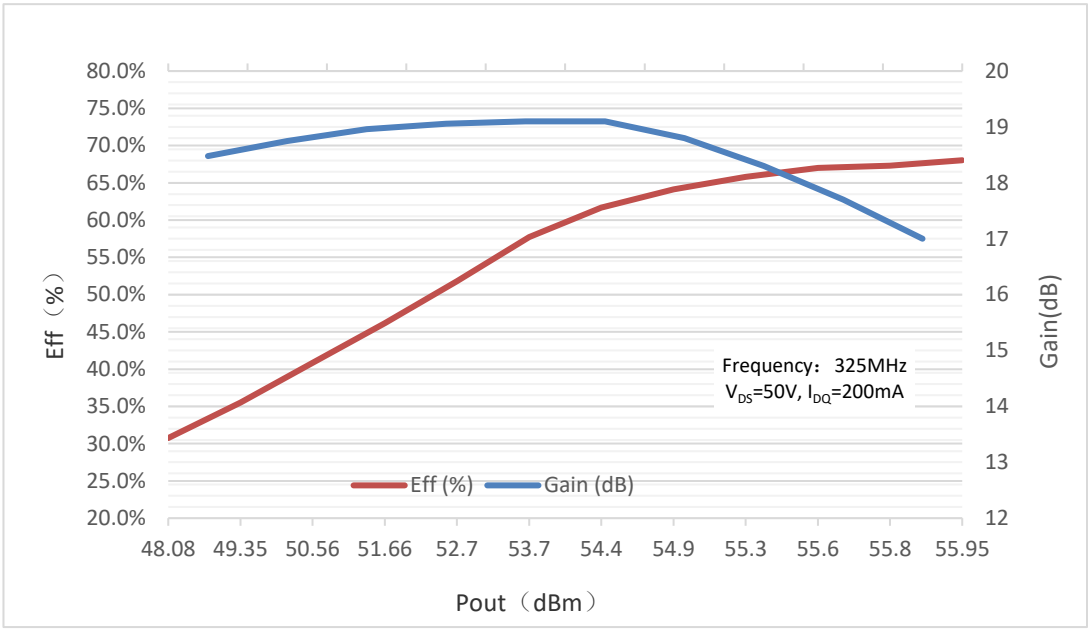


Figure 2: Power Gain and Drain Efficiency as Function of CW Power (325M)

400-460MHz
Reference Circuit of Test Fixture Assembly Diagram

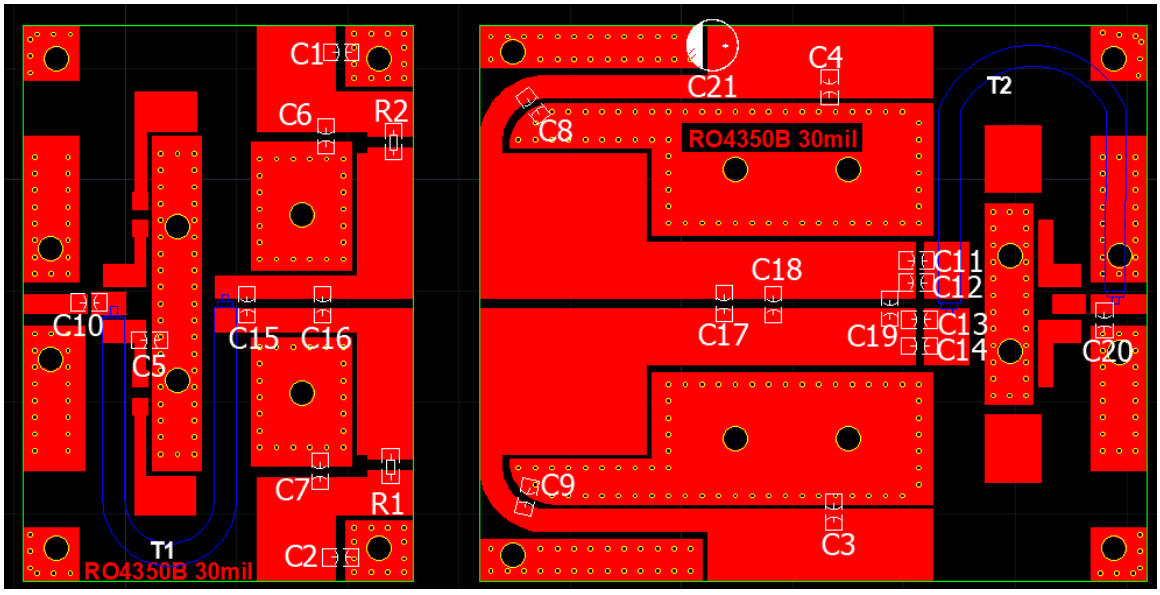


Figure 3. Test Circuit Component Layout (325M)

Table 2. Test Circuit Component Designations and Values (400-460M)

Component	Description	Suggestion
C1~C5	10uF/200V-1210	Ceramic multilayer capacitor
C6,C7	200pF	
C8，C9	560pF	
C10~C14	47pF	
C15	18pF	
C16	5.1pF	
C17	4.3pF	
C18,C20	0.5pF	
C19	6.8pF	
C21	470uF/63V	Electrolytic Capacitor
T1	25ohm-60mm	RFSFBU-086-25
T2	35ohm-65mm	SFF-35-3
R1,R2	10Ω-1206	chip resistor

TYPICAL CHARACTERISTICS

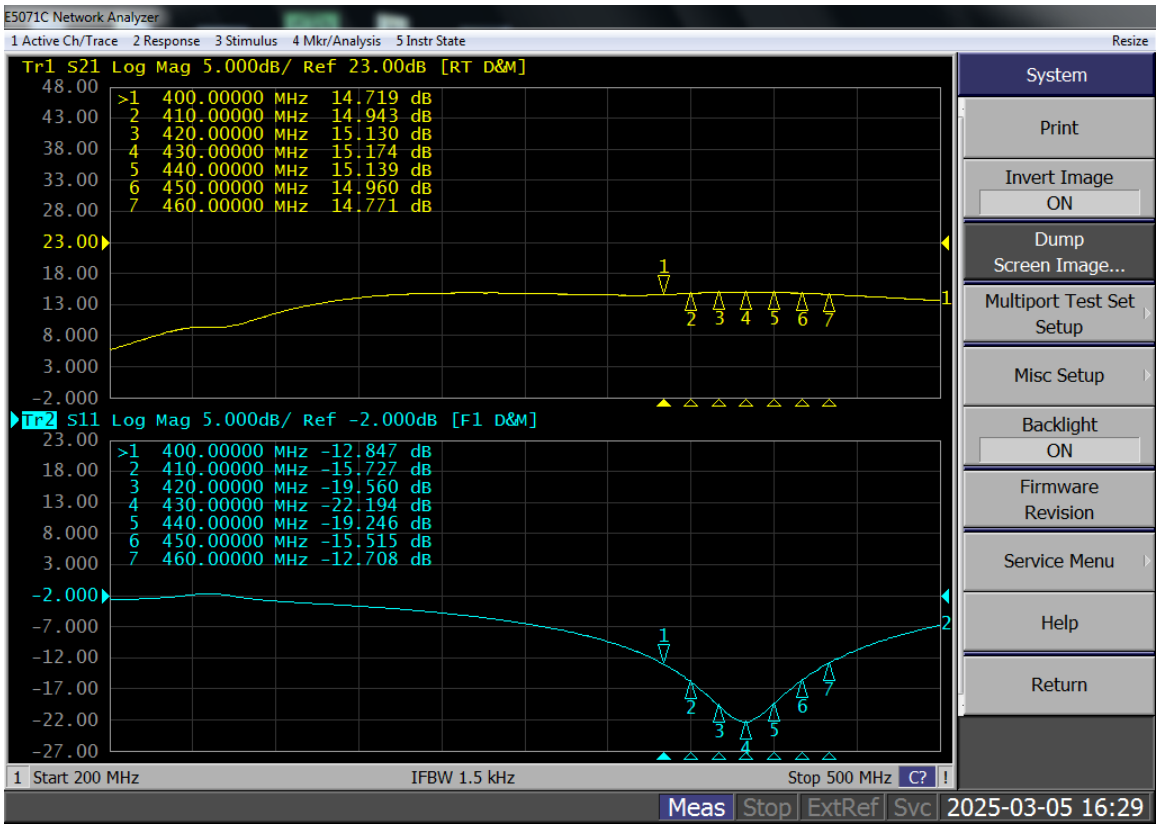
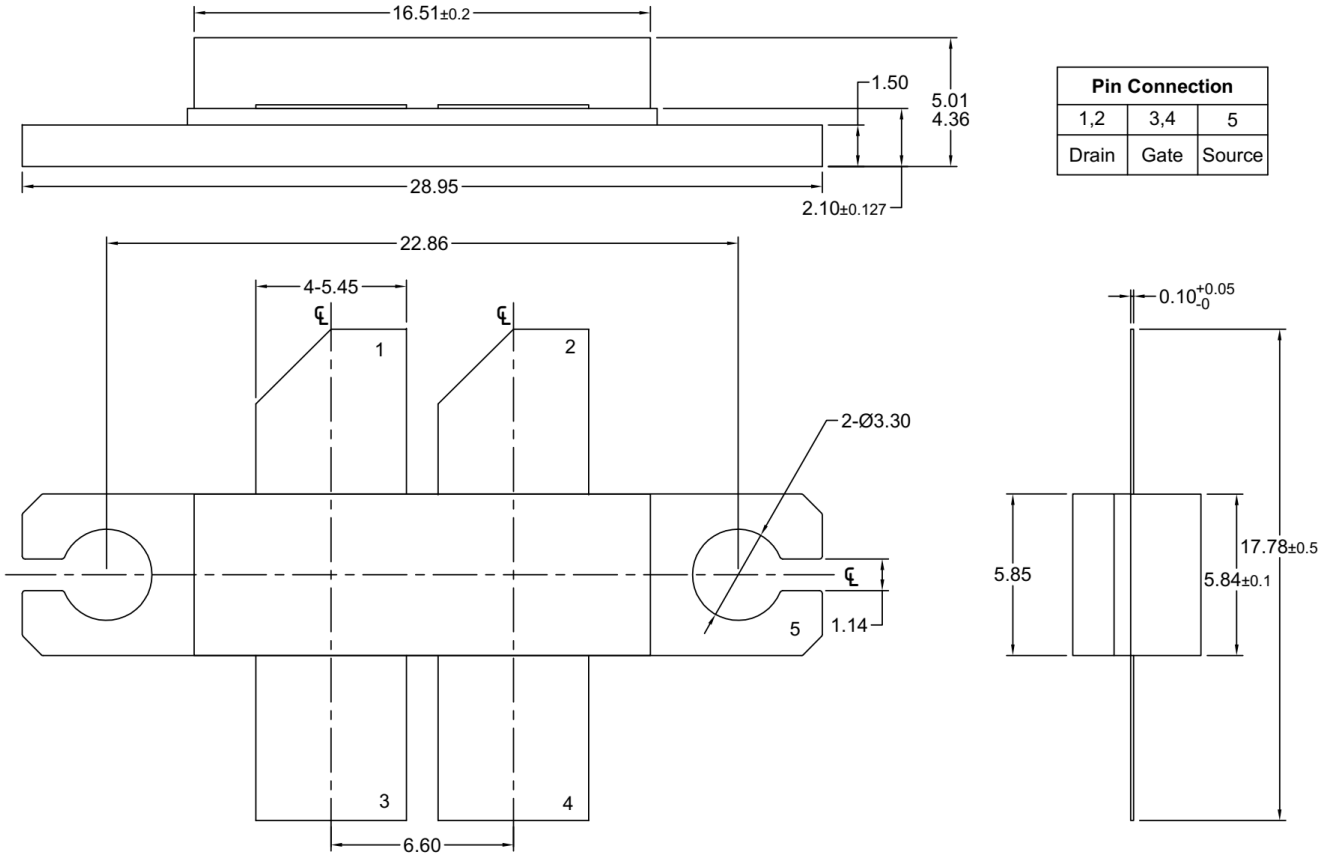


Figure 3: Network analyzer output S11/S21

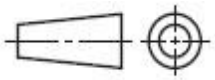
Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



Pin Connection		
1,2	3,4	5
Drain	Gate	Source

Unit：mm
Tolerances(unless specified)：x.x ±0.15
x.xx ±0.127

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-LBB					**11/15/2019**

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2019/11/15	Rev 1.0	Preliminary Datasheet Creation
2024/7/6	Rev 1.1	Modify the typo of breakdown voltage
2025/3/7	Rev 1.2	Add 400-470MHz application data, remove 500MHz result

Application data based on TC-25-12

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