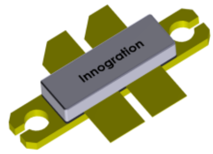
MX0565VPX LDMOS TRANSISTOR

Document Number: MX0565VPX
Preliminary Datasheet V1.0

650W, 50V High Power RF LDMOS FETs

MX0565VPX



Description

The MX0565VPX is a 650-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 0.5 GHz. It can be used for both CW and pulse applications.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.

- Typical performance(on 325MHz test board with device soldered):
  V_{DD} = 50 Volts, I_{DQ} = 200 mA, Pulsed CW.(100us,10%), Vgs=3.24V, Vds=50V,Idq=230mA

Freq (MHz)	P3dB (W)	Gain (dB)	Eff (%)
325	670	15.5	68

- Recommended driver: MR2002VP or MU1503V
- Application board for 2-30/27/40/225/325MHz upon request

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+135	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	0.22	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class

Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0Ma	$V_{(BR)DSS}$		135		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	V_{GS}(th)	——	2.65	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 230 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.24	——	V
Drain source on state resistance (Vds=0.1V, Vgs=10V)	Rds(on)		160		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{ISS}		295		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{OSS}		75		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{RSS}		1.3		pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 230 mA, f = 350MHz, pulse width:100us, duty cycle:10%

Load 10:1 All phase angles, at 650W Pulsed CW Output Power	No Device Degradation

Reference Circuit of Test Fixture Assembly Diagram

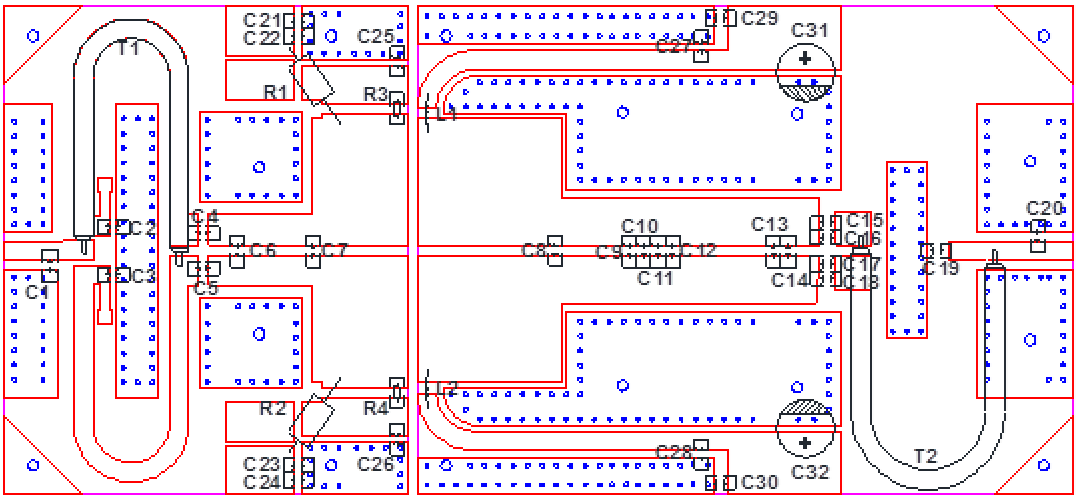


Figure 1. Test Circuit Component Layout (325M)

Table 1. Test Circuit Component Designations and Values (325MHz)

Component	Description	Suggested Manufacturer
C1,	20 pF	ATC800B
C2, C3, C4, C5, C15, C16, C17, C18, C22, C23, C27, C28	470 pF	ATC800B
C6, C11, C12, C13	10 pF	ATC800B
C7, C8, C9, C10, C14,	18 pF	ATC800B
C19, C20	4.7 pF	ATC800B
C21, C24, C25, C26, C29, C30	Ceramic multilayer capacitor, 10uF, 100V	
R1, R2	270 Ω, 1/4W	
R3, R4	13 Ω	1206
L1, L2	30nH Air core inductance	
C31, C32	Electrolytic Capacitor ,470uF,63V	
PCB	0.508mm [0.020''] thick, εr=3.48, Rogers RO4350B, 1 oz. copper	

TYPICAL CHARACTERISTICS

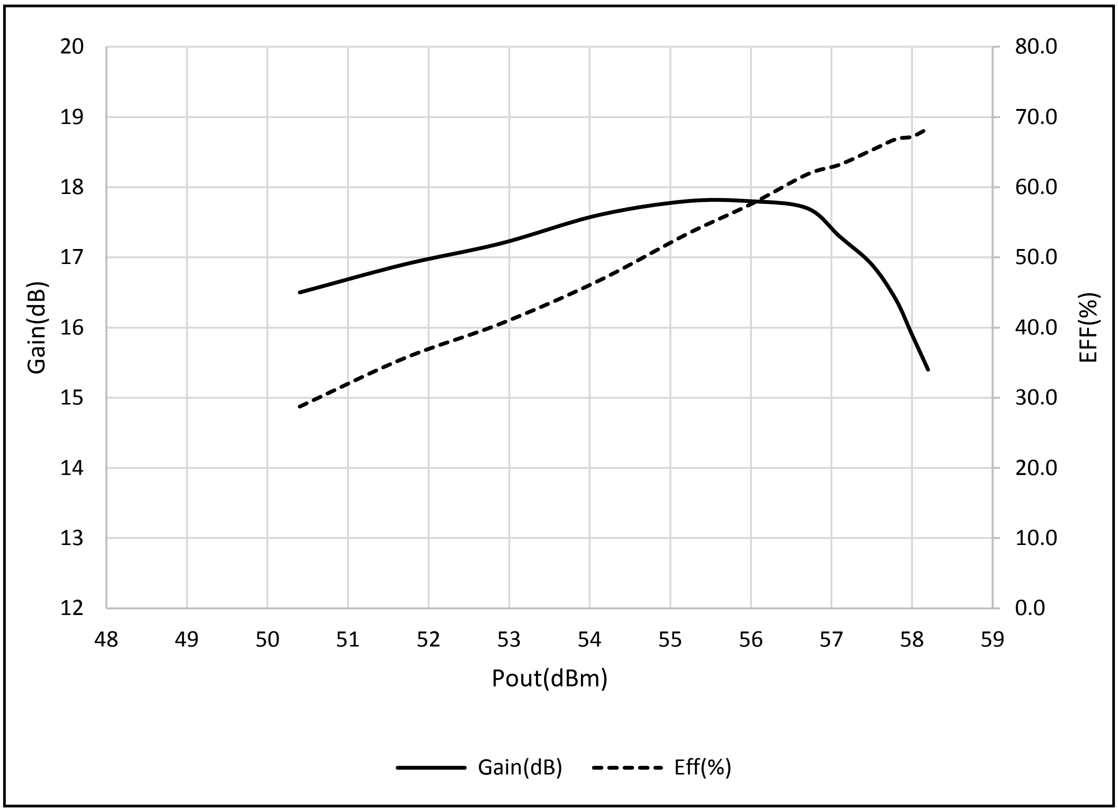
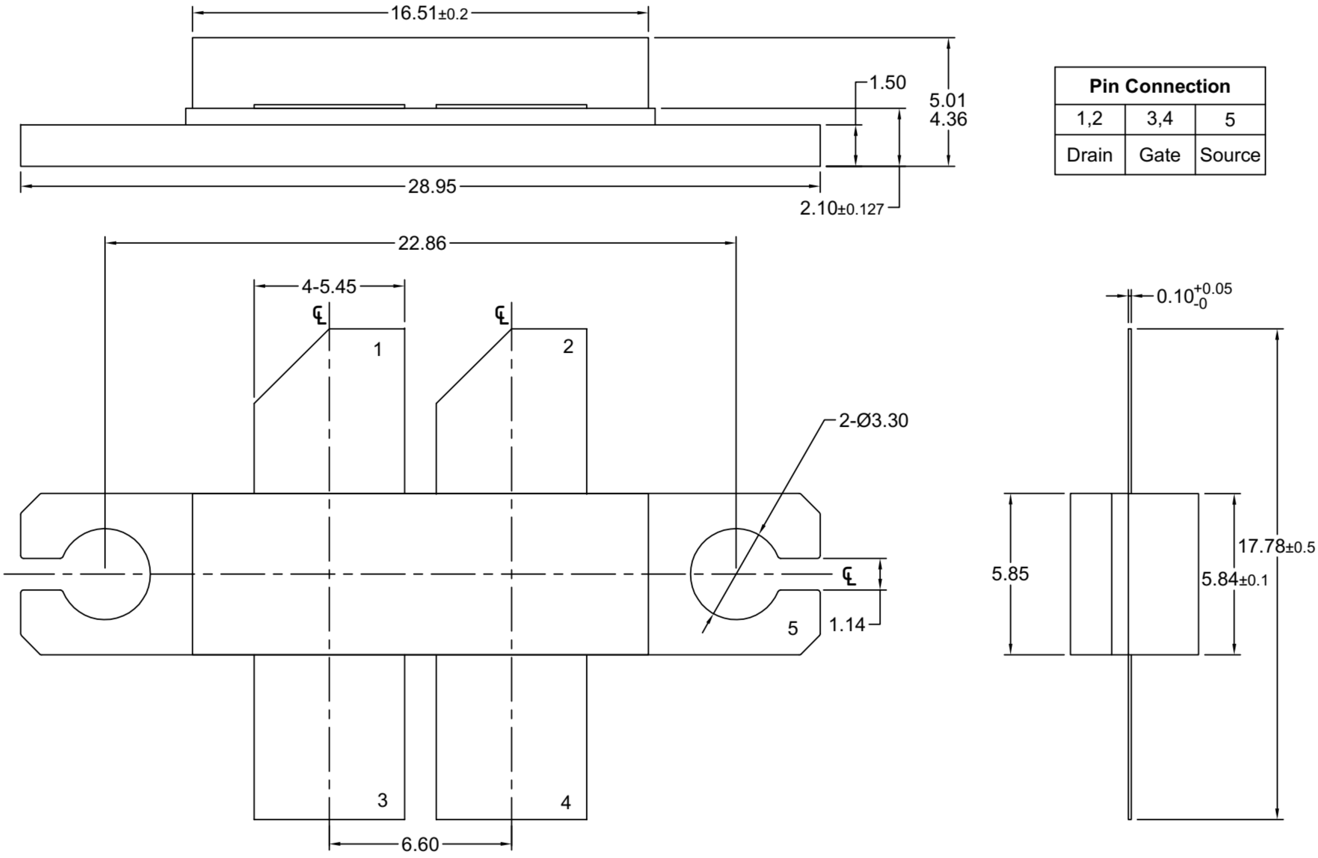


Figure 2: Power Gain and Drain Efficiency as Function of Pout (325MHz)

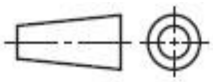
Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



Pin Connection		
1,2	3,4	5
Drain	Gate	Source

Unit: mm
Tolerances(unless specified): x.x ±0.15
x.xx ±0.127

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-LBB					**11/15/2019**

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2019/12/17	Rev 1.0	Preliminary Datasheet Creation

Disclaimers