



700-1700MHz, 45W, 28V High Power RF LDMOS FETs

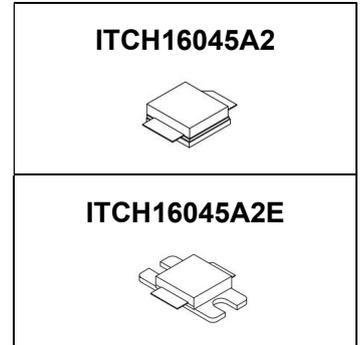
Description

The ITCH16045A2 is a 45-watt, input-matched LDMOS FETs, designed for Beidou Global Positioning System and communication/ISM applications with frequencies from 700 to 1700 MHz. It can be used in Class AB/B and Class C for all typical modulation formats.

- Typical Performance (On Innegration fixture with device soldered):

$V_{DD} = 28$ Volts, $I_{DQ} = 50$ mA, CW.

Frequency	Gp (dB)	P_{-1dB} (W)	$\eta_D@P_{-1}$ (%)
1615 MHz	20	43	64.5



Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCl drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c = 85^\circ\text{C}$, $T_j = 200^\circ\text{C}$, DC test	$R_{\theta JC}$	0.7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}			100	μA
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}			1	μA
Gate--Source Leakage Current ($V_{GS} = 10\text{V}$, $V_{DS} = 0\text{V}$)	I_{GSS}			1	μA



Gate Threshold Voltage ($V_{DS} = 28V, I_D = 300 \mu A$)	$V_{GS(th)}$		1.75		V
Gate Quiescent Voltage ($V_{DD} = 28V, I_D = 50mA$, Measured in Functional Test)	$V_{GS(Q)}$		1.9		V

Functional Tests (In Innegration Test Fixture, 50 ohm system) $V_{DD} = 28Vdc, I_{DQ} = 50mA, f = 1615MHz$, CW Signal Measurements.

Power Gain	G_p		20		dB
1 dB Compression Point	P_{-1dB}		43		W
Drain Efficiency@P1dB	η_D		64.5		%
Input Return Loss	IRL		-10		dB

Load Mismatch (In Innegration Test Fixture, 50 ohm system): $V_{DD} = 28Vdc, I_{DQ} = 50mA, f = 1615MHz$

VSWR 10:1 at 50W pulse CW Output Power	No Device Degradation
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TYPICAL CHARACTERISTICS

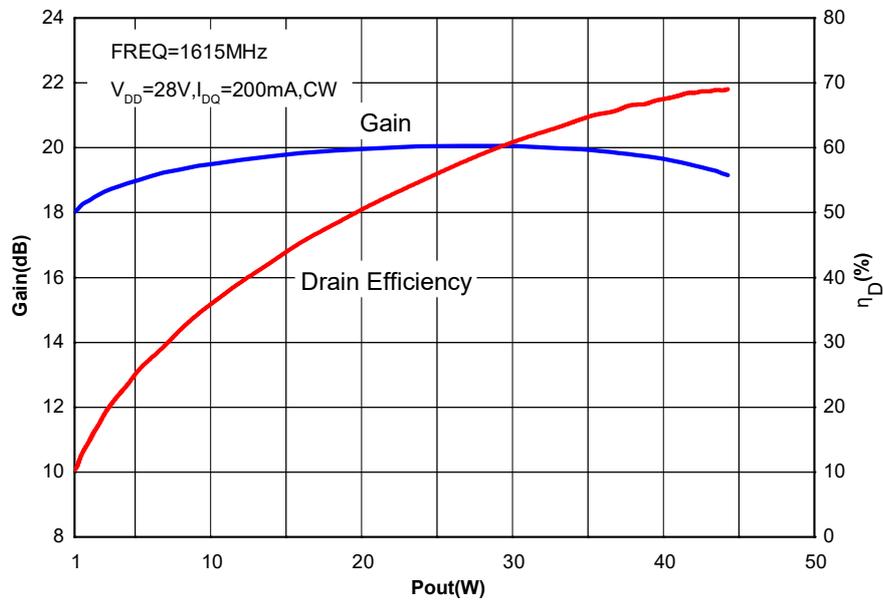
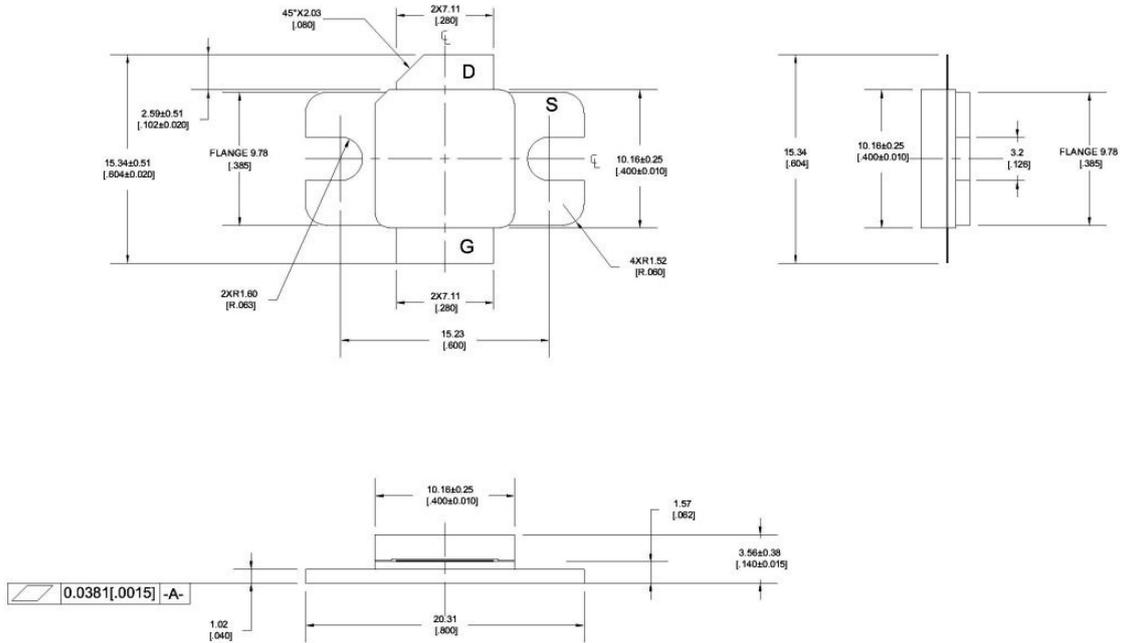


Figure 1. Power gain and drain efficiency as function of average load power



Package Outline

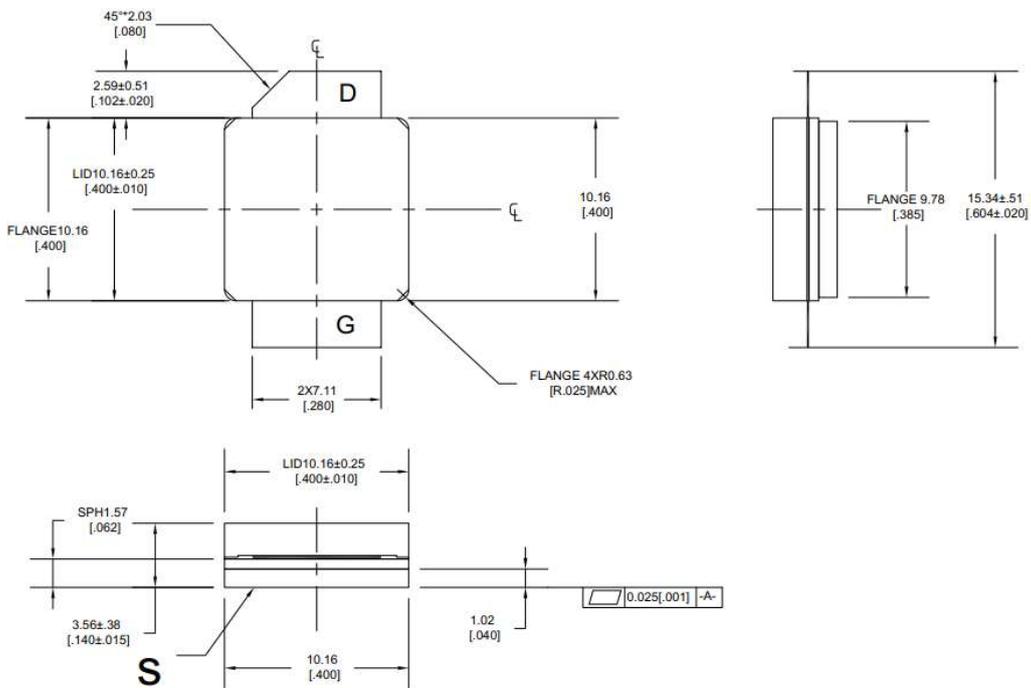
Eared Flanged ceramic package; 2 leads (A2E)



Unit: mm [inch]

Tolerance .xx +/- 0.01 .xxx +/- 0.005 inches

Earless Flanged ceramic package; 2 leads (A2)



Unit: mm [inch]

Tolerance .xx +/- 0.01 .xxx +/- 0.005 inches



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2016/12/26	Rev 1.0	Preliminary Datasheet
2017/03/17	Rev 2.0	Preliminary Datasheet
2020/6/21	Rev 2.1	Modify the lower frequency limits

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