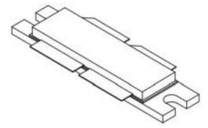
MQ1470VP LDMOS TRANSISTOR

750W, 50V High Power RF LDMOS FETs

MQ1470VP



Description

The MQ1470VP is a 750W P1dB (900W P3dB), high performance, internally matched LDMOS FET, designed for avionics applications with frequencies 1.2 to 1.4GHz

It is featured for high power and high ruggedness.

It is recommended to use this device under pulse condition only

- Typical Pulse Performance (on innogration wide band test fixture with device soldered):
  Vds = 50 V, Idq = 50 mA, TA = 25 °C

Freq(MHz)	Pin(dBm)	P3dB(dBm)	P3dB (W)	IDS(A)	Gain(dB)	Eff(%)
1200	47	60.3	1072	4.06	13.3	53.50
1300	48.1	60.2	1047	4.23	12.1	50.15
1400	46.4	59.86	968	3.95	13.46	49.71

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case,Case Temperature 80°C, 870W Pout, Pulse width: 100us, duty cycle: 10%, Vds=50 V, I_{DQ} = 100 mA	$R_{\theta JC}$	0.02	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit

DC Characteristics

Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	115			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}			10	µA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			1	µA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 uA)	$V_{GS(th)}$		1.6		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_{DQ} = 50 mA, Measured in Functional Test)	$V_{GS(Q)}$		3		V

Functional Tests (In Innogration test fixture, 50 ohm system) : Pulse CW Signal Measurements. (Pulse Width=100s, Duty cycle=10%), Pin=46dBm

Power Gain @ Pout	G_p		13.3		dB
1dB compressed point	P1dB	750	800		W
Drain Efficiency@Pout	η_D		45.0		%
Input Return Loss	IRL		-7		dB

Reference Circuit of Test Fixture

(Layout file upon request)   PCB: Roger 4350B, 20mils

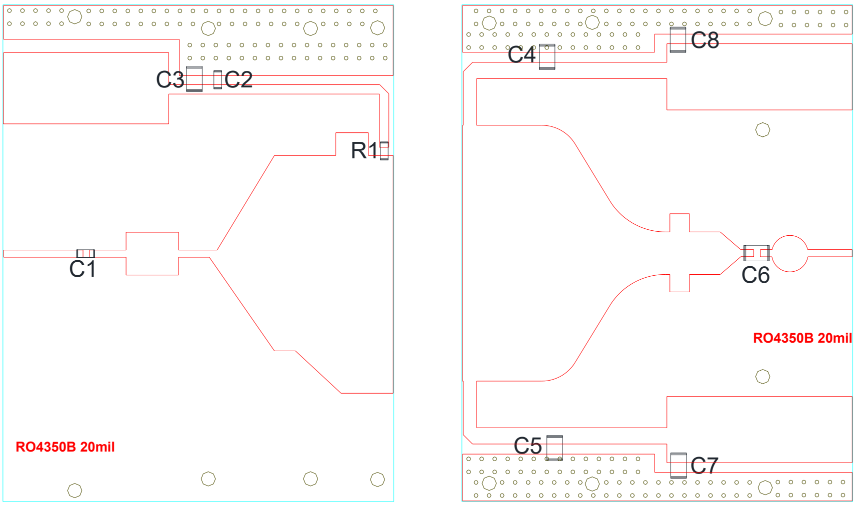


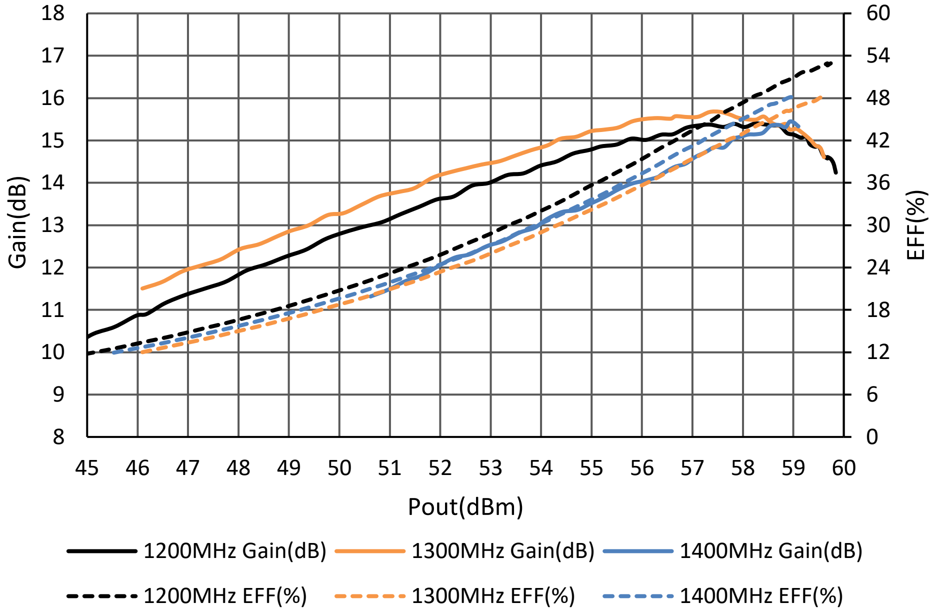
Figure 1.   Test Circuit Component Layout

Part	description	Model
C1,C2	56pF	ATC600F
C4,C5,C6	47pF	ATC800B
C3,C7,C8	10uF	10uF/50V
R1	13Ω	1206

TYPICAL CHARACTERISTICS

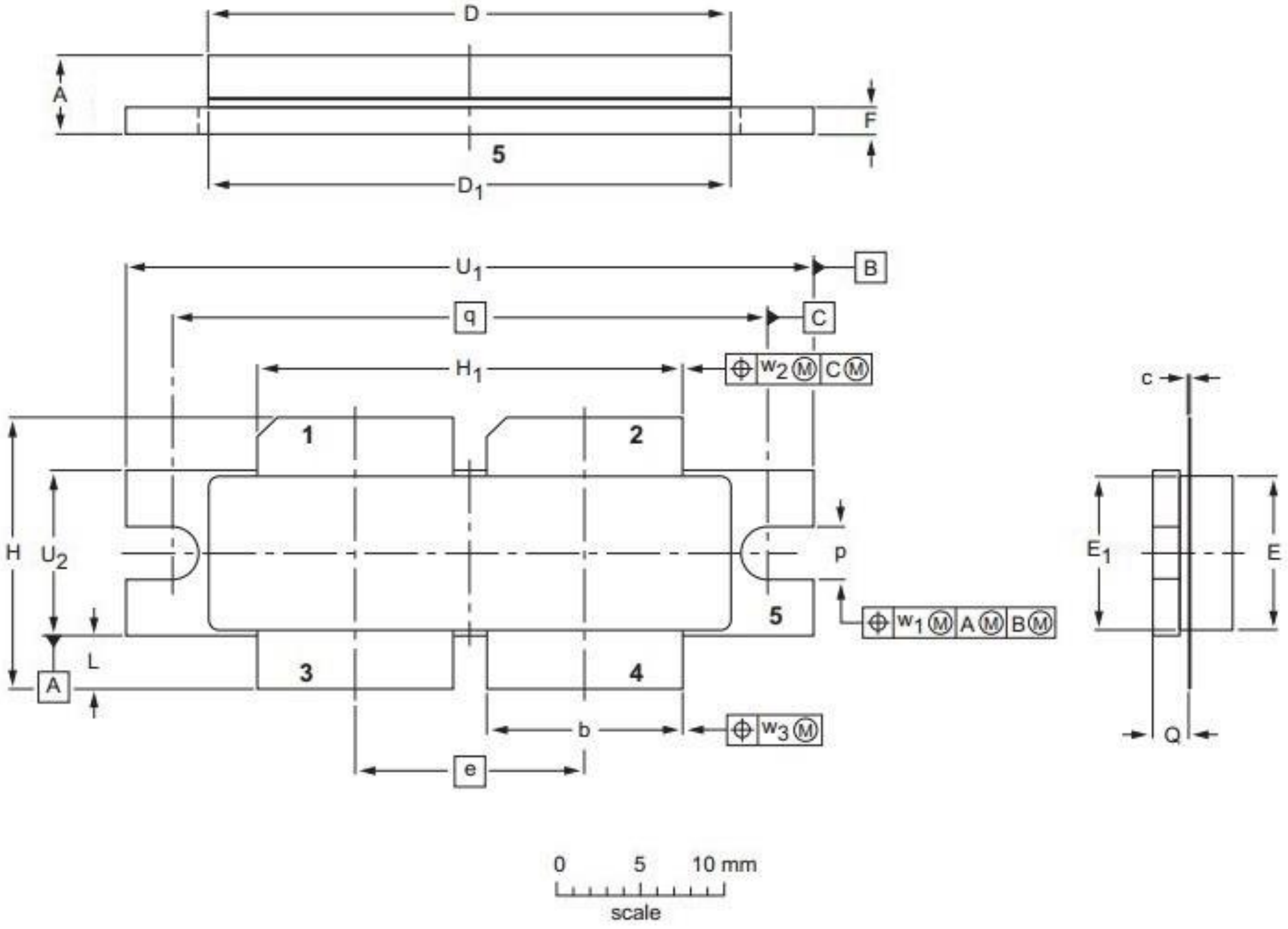
Pulse width:100uS, duty cycle: 10%, Vds = 50 V, Idq = 100 mA, TA = 25 °C

Figure 2: Power gain and Efficiency as a Function of Pout

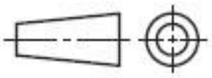


Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D₁	e	E	E₁	F	H	H₁	L	p	Q	q	U₁	U₂	W₁	W₂	W₂
Mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
Inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					**03/12/2013**

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2018/8/4	Rev 1.0	Preliminary Datasheet Creation
2019/11/29	Rev 1.1	Update PCB layout
2025/10/3	Rev 1.2	Deleting the misleading graph of S21/S11

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