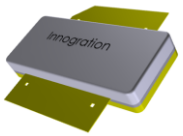
MC1275VS LDMOS TRANSISTOR

Document Number: MC1275VS
Preliminary Datasheet V1.0

750W/900W, 50V High Power RF LDMOS FETs

MC1275VS



Description

The MC1275VS is single ended 50V LDMOS, internally matched for pulse applications operating **over 1030 to 1090 MHz at power 900W** and can be used **over the 960 to 1215 MHz band at reduced power 750W.**

It is suitable for use in commercial pulse applications with large duty cycles and long pulses, such as IFF, secondary surveillance radars, ADS--B transponders, DME and other complex pulse chains.

Special note:

With 2 pieces of MC1275VS in form of push pull pairs, it can output 1700W over either 1030 to 1090MHz, or output 1400W over 960-1215MHz, as leading output capability while in highly compact PCB area.

- Typical performance(on 960-1215MHz application board with devices soldered)

V_{DS}=50V,Idq=100mA, Pulsed CW, 10% duty cycle, 128us pulse width

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
960	58.56	718.3	56.5	16.7	59.17	825.4	56.9
1030	59.22	836.4	54.8	17.51	60.24	1056.7	57.8
1090	59.45	881.0	55.4	16.83	60.27	1064.8	57.2
1150	59.22	834.8	58.8	16.48	59.94	987.1	60.0
1215	58.29	675.1	59.5	17.09	59.1	813.6	61.0

V_{DS}=52V,I_{DQ}=100mA

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
960	58.91	778.5	57.0	16.82	59.49	889.7	57.0
1030	59.64	920.8	55.7	17.55	60.56	1138.5	58.4
1090	59.72	938.6	55.0	16.8	60.53	1129.6	56.6
1150	59.55	901.5	58.5	16.56	60.25	1059.1	59.7
1215	58.67	736.2	59.5	17.21	59.45	880.2	60.7

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc

Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Pulse: Case Temperature 75 C, 900 W Peak, 128 usec Pulse Width, 10% Duty Cycle, 50 Vdc, 1030 MHz	$R_{\theta JC}$	0.03	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	115			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}			10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 uA)	$V_{GS(th)}$		1.6		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_{DQ} = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$		3		V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 100 mA, f = 1030MHz, pulse width:128us, duty cycle:10%,

VSWR: > 7:1 at All Phase Angles	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 1: Pulsed CW Gain and Power Efficiency as a Function of Pout within 960-1215MHz at different drain voltage

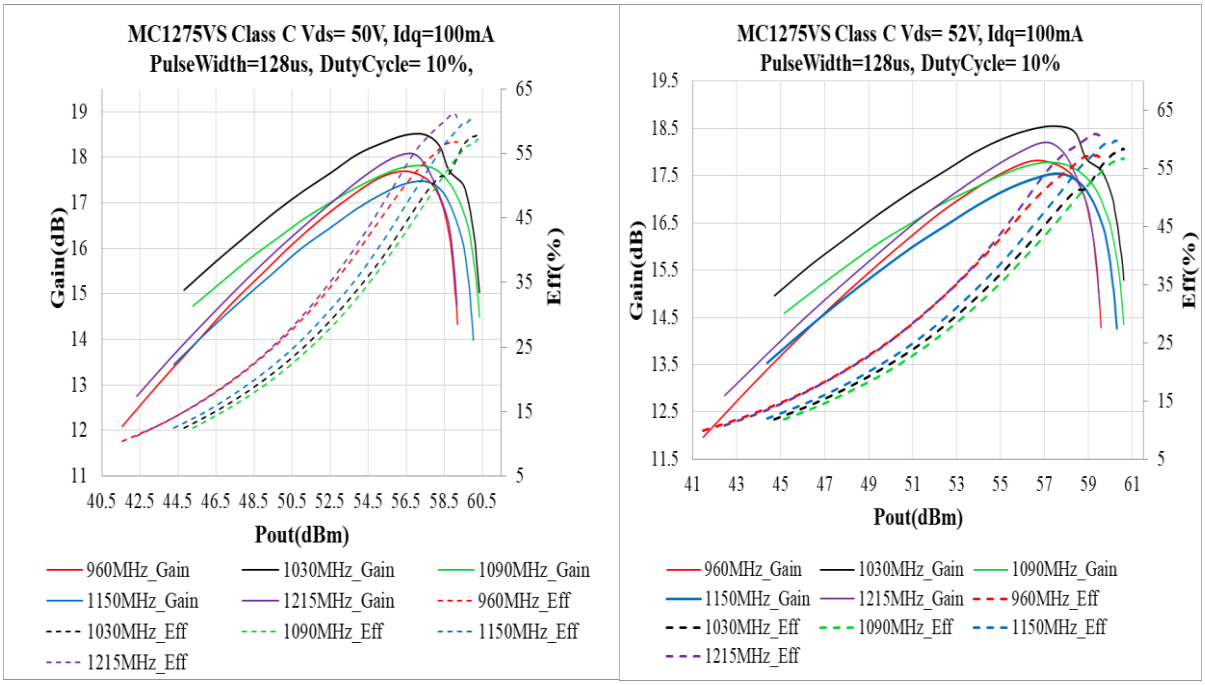
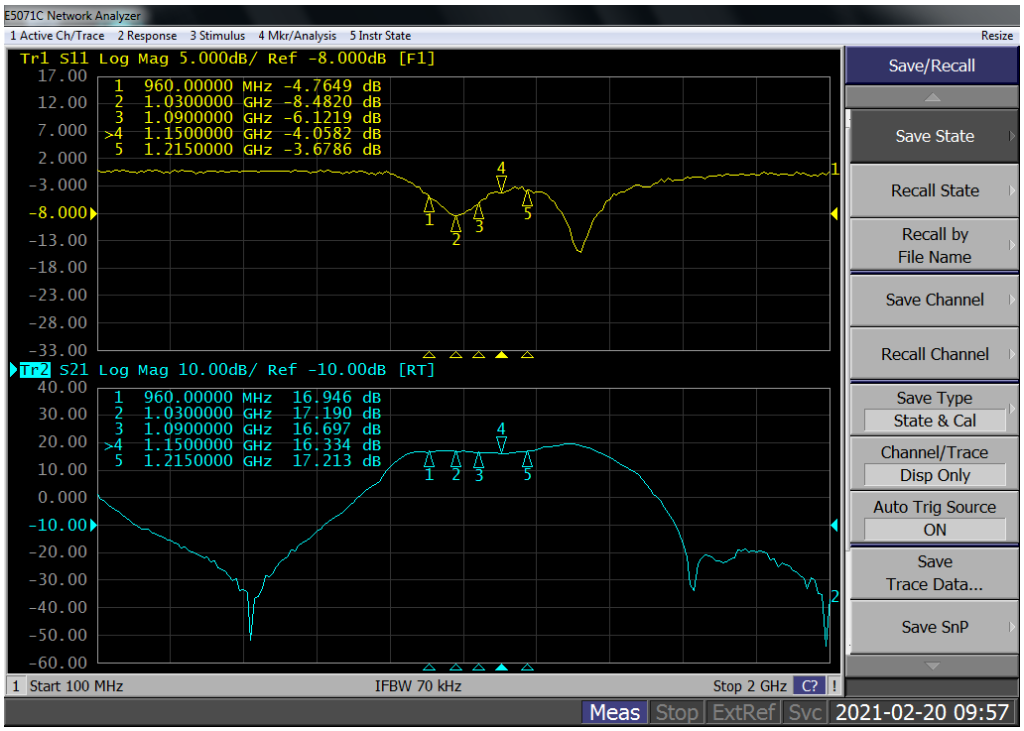


Figure 2: Network analyzer output S11/S21 at 50V Idq=1.5A



Reference Circuit of Test Fixture Assembly Diagram

(Layout file upon request, 30mil RO4350)

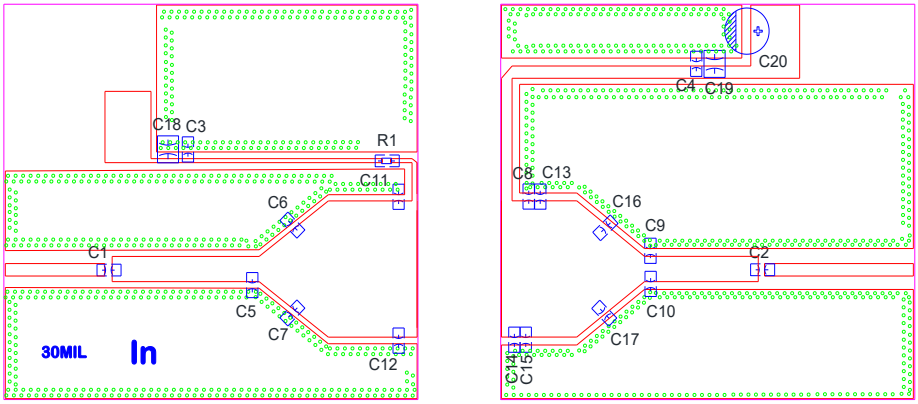


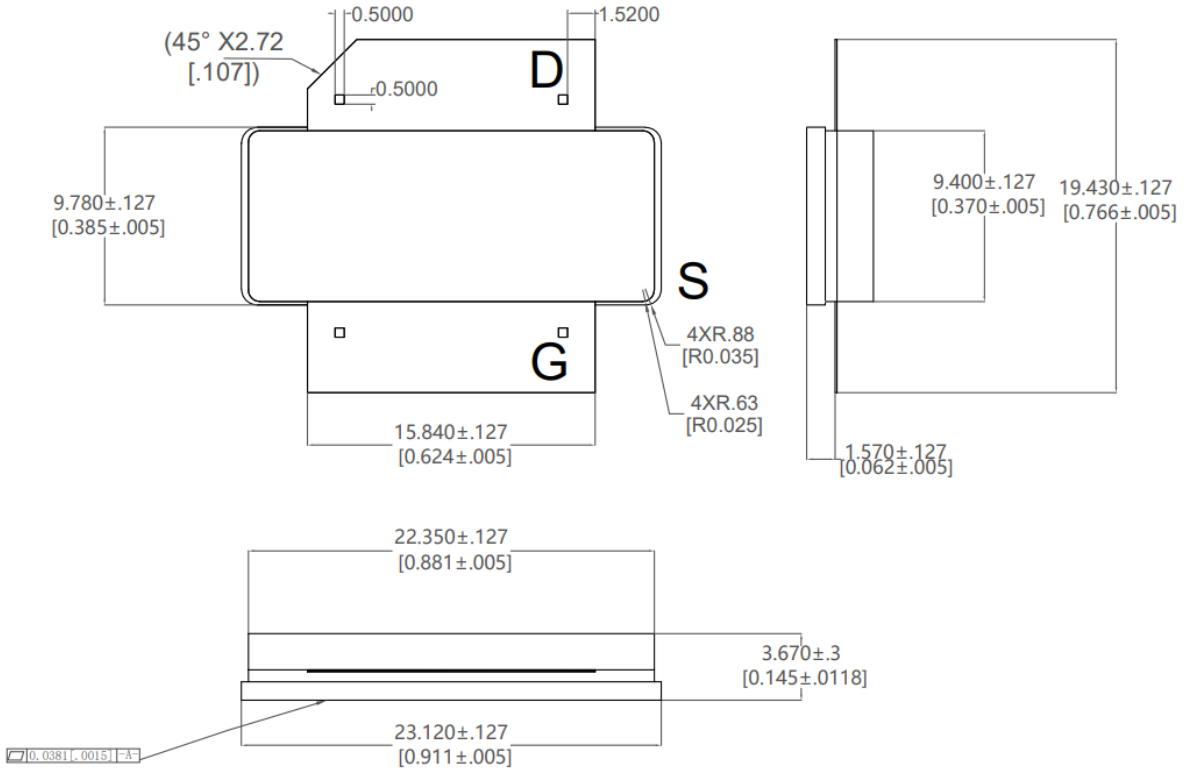
Table 5. Test Circuit Component Designations and Values

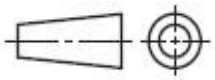
Designator	Comment	Footprint	Quantity
C1,C2, C3, C4	33pF	0805	4
C5, C6, C7, C8, C9, C10	2.0pF	0805	6
C11, C12	6.8pF	0805	2
C13, C14, C15	4.3pF	0805	3
C16, C17	1.0pF	0805	2
C18, C19	10uF/100V	1210	2
C20	1000uF/63V		1
R1	10ohm	0603	1

Package Outline

Flangeless ceramic package;

INP-688-2-EL（C2)



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					**09/27/2018**

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/2/20	Rev 1.0	Preliminary datasheet

Application data based on LSM-21-03

Disclaimers