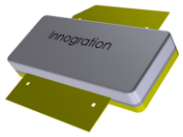
MC1225S LDMOS TRANSISTOR

Document Number: MC1225S
Product Datasheet V1.0

250W, Avionics High Power RF LDMOS FETs

MC1225S



Description

The MC1225S is a 250-watt, internally matched, single ended LDMOS FETs, designed for avionics application within 960-1220MHz. It can be used in Class AB/B and Class C for any pulse and CW signal.

•Typical Performance (On Innogration fixture with device soldered):

V_{DD} = 28 Volts, I_{DQ} = 200 mA, Pulsed CW, 10% 100uS

Freq (MHz)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (W)	P3dB Eff(%)
960	226.5	59	15.26	256	60
1090	222.7	55	15.75	252	56
1220	212.0	54	16.58	250	56

V_{DD} = 32 Volts, I_{DQ} = 500 mA, CW.

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	IDS(A)	Power Gain(dB)	Eff(%)
960	40.7	54.9	309.0	16.9	14.2	57.143
1030	39.6	54.4	275.4	15.7	14.8	54.821
1090	39.5	54.5	281.8	16.7	15	52.739
1160	39.8	54.5	281.8	17.6	14.7	50.042
1220	38.1	54.1	257.0	15.9	16	50.519

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- L band avionics pulse or CW amplifier
- ISM applications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65V, V_{GS} = 0 V)	I_{DSS}			100	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}			1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 450 μA)	$V_{GS(th)}$		1.9		V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$		2.72		V
Functional Tests (On Demo Test Fixture, 50 ohm system) V_{DD} = 32 Vdc, I_{DQ} = 200 mA, f = 1220 MHz, Pulse CW Signal Measurements.					
Power Gain	Gp		14		dB
Drain Efficiency@P1dB	η_D		50		%
3 dB Compression Point	P_{-3dB}	250			W
Input Return Loss	IRL		-4		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 32 Vdc, I_{DQ} = 200 mA, f = 1220 MHz

VSWR 10:1 at 250W pulse CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 1. Power Gain and Drain Efficiency as Function of Pulse Output Power

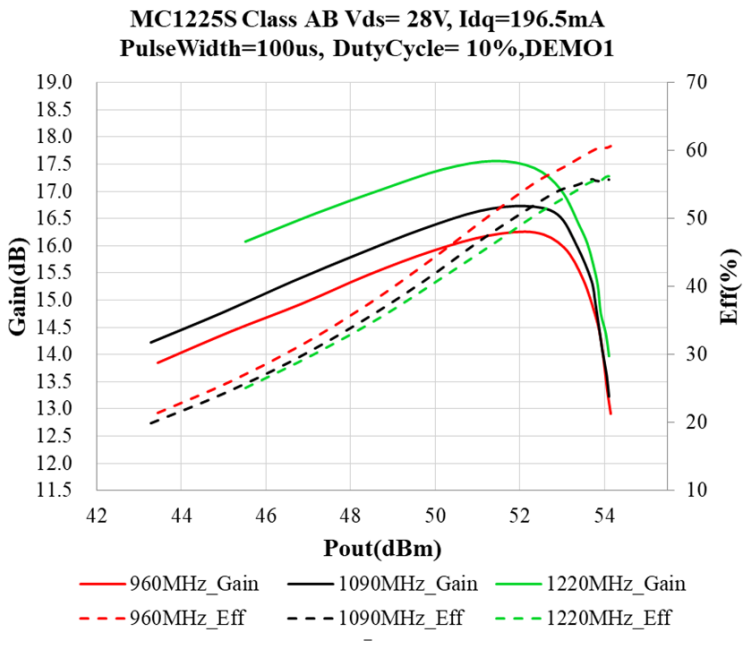


Figure 2. Network analyzer output S11/S21 (VDS=32V IDQ=500mA VGS=2.9V)

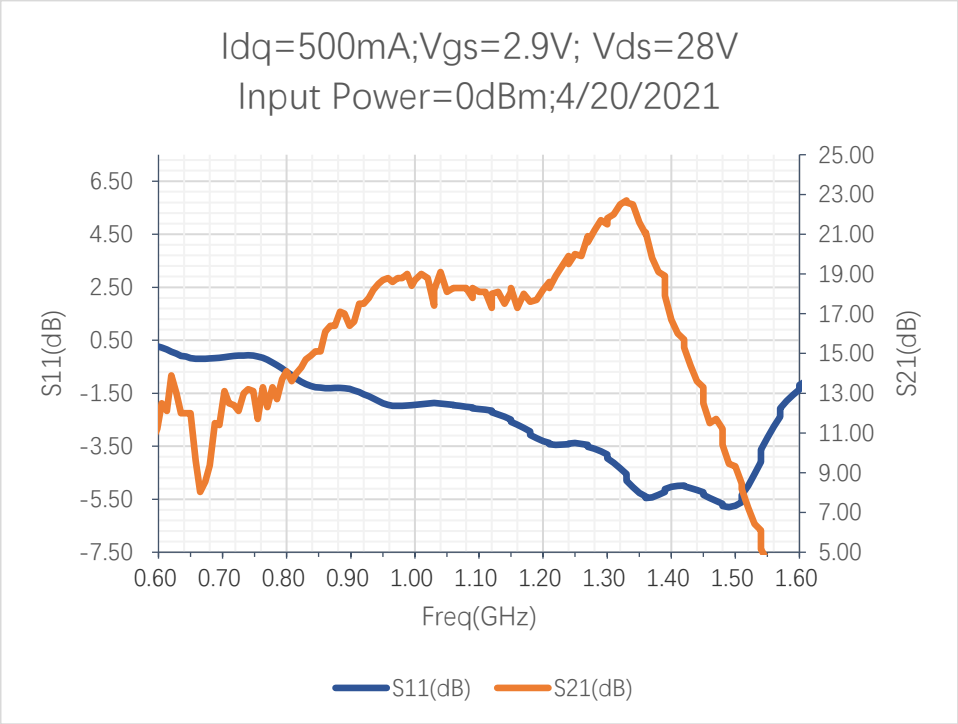


Figure 3. Test Circuit Component Layout

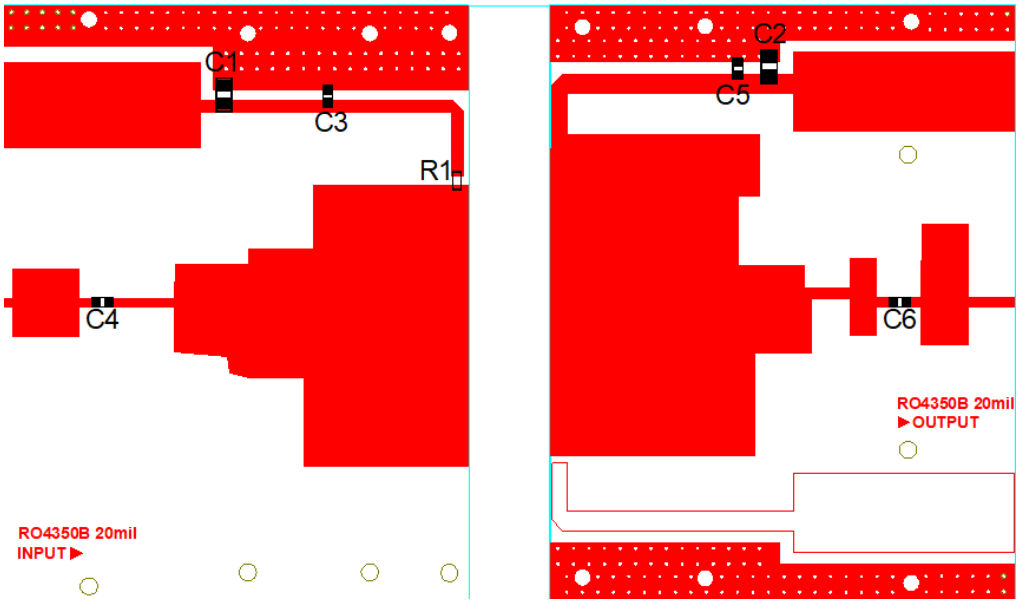


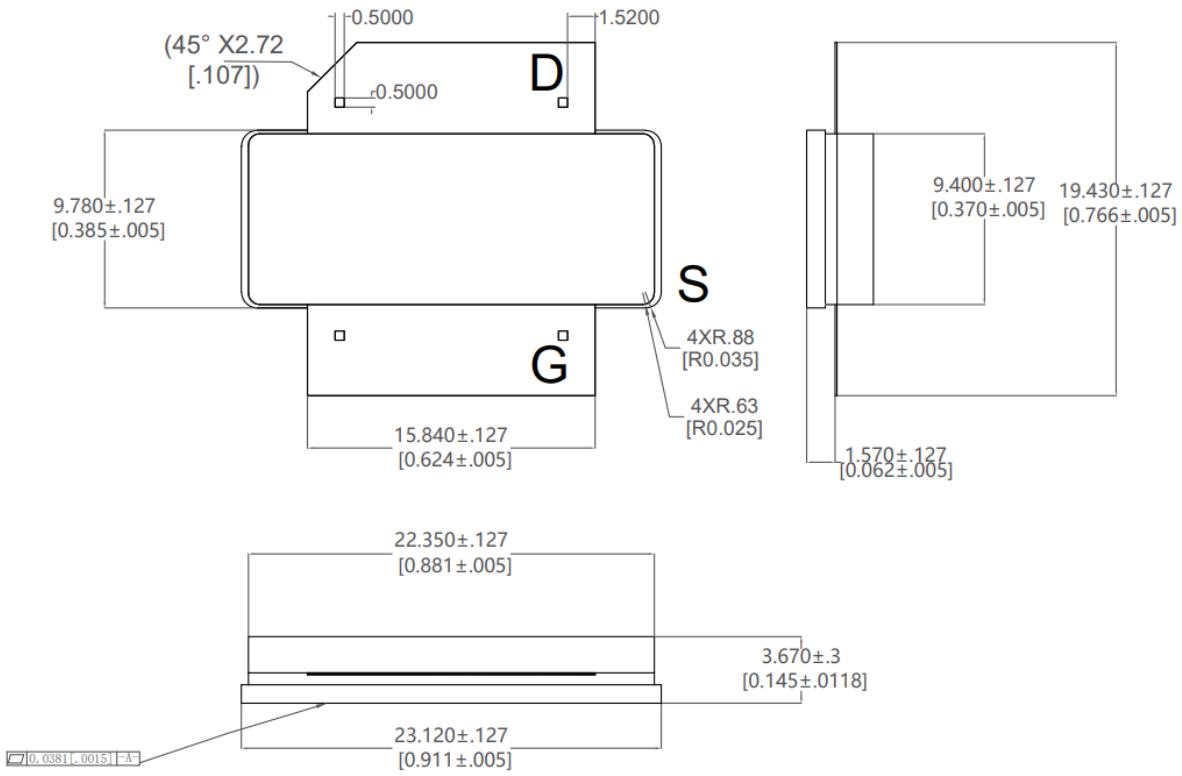
Table 4. Test Circuit Component Designations and Values

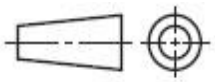
Component	Description	Suggested Manufacturer
C1,C2	Ceramic multilayer capacitor, 10uF, 100V	10uF/100V
C3,C4,C5,C6	33pF	ATC800B
R1	Chip Resistor,9.1Ω,1206	
PCB	20mil thickness, εr=3.5, Ro4350B, 1 oz. copper	

Package Outline

Flangeless ceramic package;

INP-688-2-EL（C2)



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/4/22	Rev 1.0	Product Datasheet

Application data based on JF-21-02

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