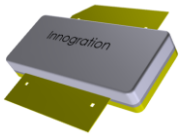
MC1450VS LDMOS TRANSISTOR

Document Number: MC1450VS
Preliminary Datasheet V1.0

500W, 1.2-1.4GHz 50V High Power RF LDMOS FETs

MC1450VS



Description

The MC1450VS is single ended 50V LDMOS, internally matched for pulse applications operating **over 1.2 to 1.4GHz at power 500W**

Special note:

With 2 pieces of MC1450VS in form of push pull pairs, it can output 1000W over 1.2 to 1.4GHz as leading output capability while in highly compact PCB area.

- Typical performance(on 1.2-1.4GHz application board with devices soldered)

V_{DS}=50V,Idq=50mA, Pulsed CW, 10% duty cycle, 10us pulse width

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1200	57.13	516.3	56.8	12.8	57.67	585.4	56.0
1250	57.53	566.5	53.8	12.56	58.2	661.2	54.2
1300	57.93	621.1	54.2	12.64	58.52	710.5	54.5
1350	57.77	597.8	54.9	12.76	58.25	667.6	54.3
1400	57.01	502.2	53.4	12.6	57.38	547.6	51.8

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Pulse: Case Temperature 75 C, 500 W Peak, 10 usec Pulse Width, 10% Duty Cycle, 50 Vdc, 1400MHz	$R_{\theta JC}$	0.04	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	115			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}			10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 uA)	$V_{GS(th)}$		1.6		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_{DQ} = 50 mA, Measured in Functional Test)	$V_{GS(Q)}$		3		V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 50 mA, f = 1400MHz, pulse width:10us, duty cycle:10%,

VSWR: > 7:1 at All Phase Angles	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 1: Pulsed CW Gain and Power Efficiency as a Function of Pout within 1.2-1.4GHz at different drain voltage

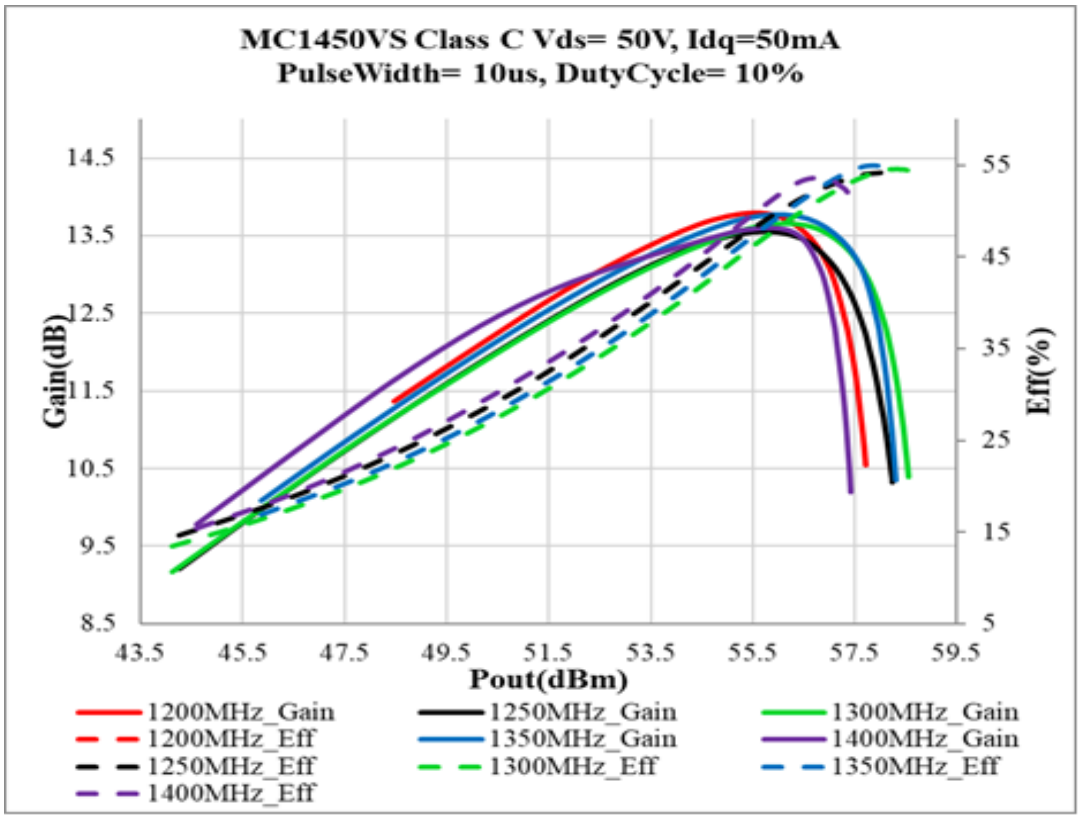
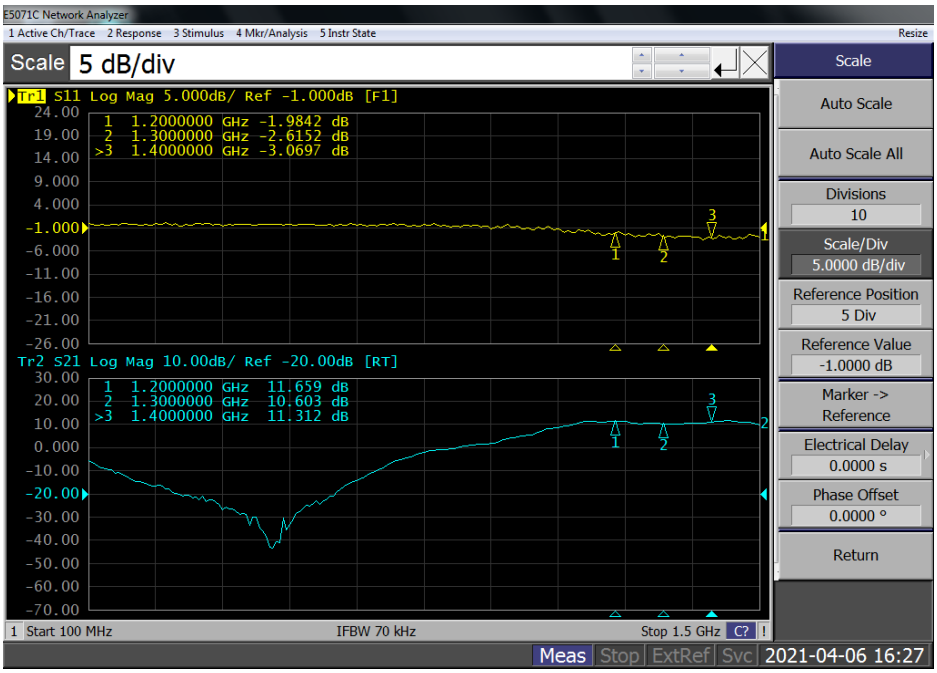


Figure 2: Network analyzer output S11/S21 at 50V Idq=1A



Reference Circuit of Test Fixture Assembly Diagram

(Layout file upon request, 30mil RO4350)

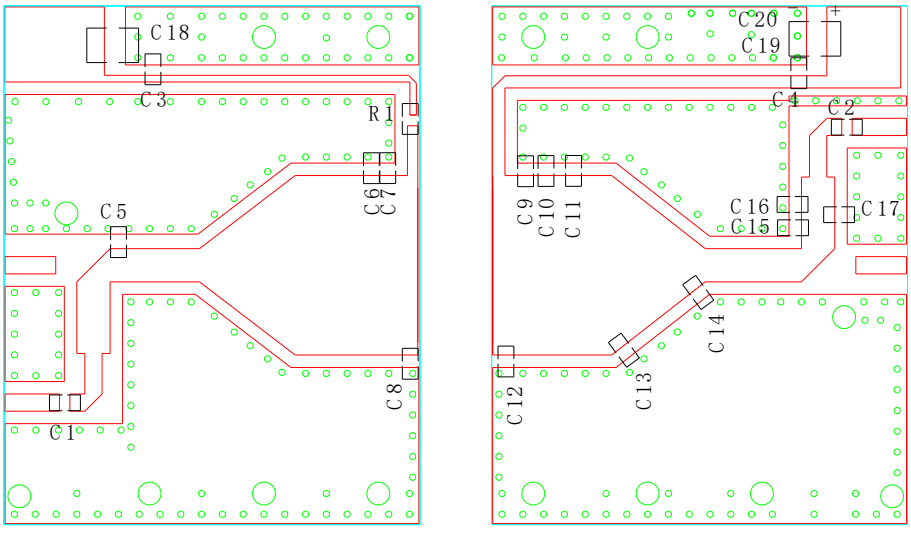


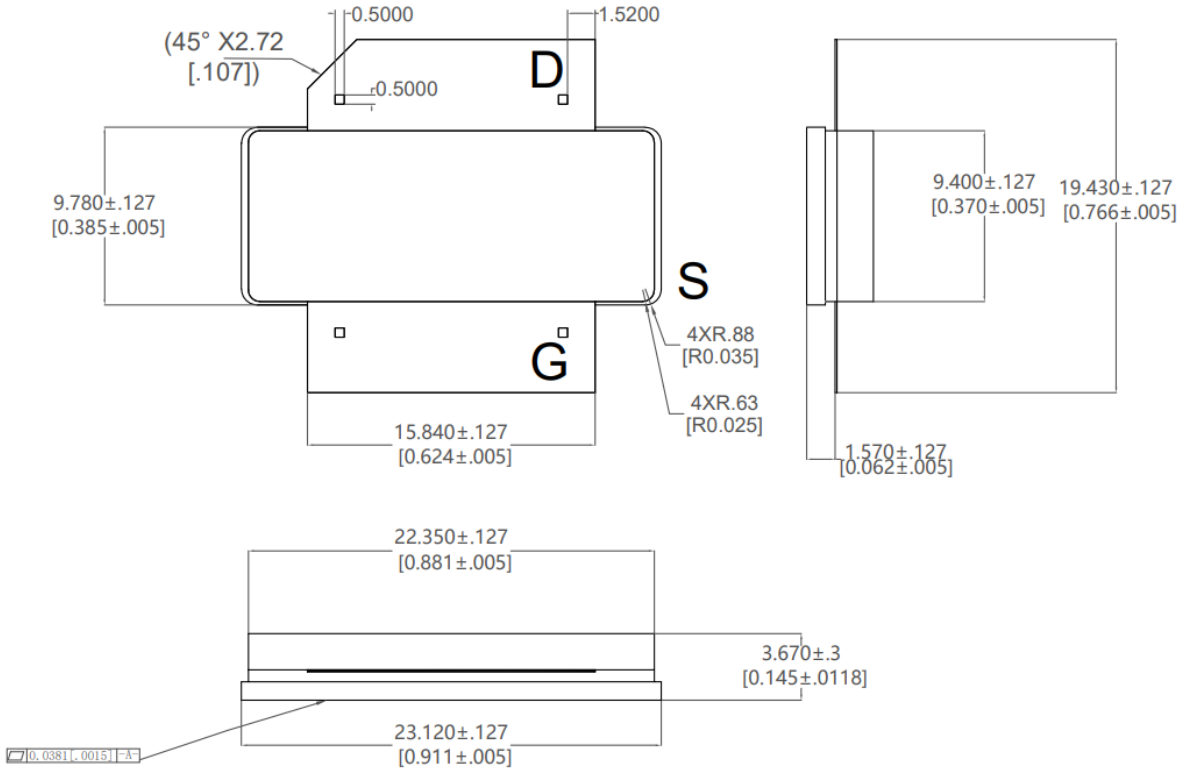
Table 5. Test Circuit Component Designations and Values

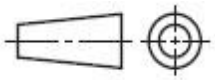
Designator	Comment	Footprint	Quantity
C1, C2, C3, C4	27pF	0805	4
C5, C6, C13, C16	2.0pF	0805	4
C7, C12, C14	6.8pF	0805	3
C8, C9, C10, C11	3.9pF	0603	4
C15	0.5pF	0603	1
C17	1.0pF	0805	1
C18, C19	10uF/100V	1210	2
C20	220uF/63V		1
R1	10ohm	0603	1

Package Outline

Flangeless ceramic package;

INP-688-2-EL（C2)



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					**09/27/2018**

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/4/6	Rev 1.0	Preliminary datasheet

Application data based on LSM-21-08

Disclaimers