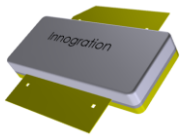
700-1000MHz, 300W, 30V High Power RF LDMOS FETs

Description

The ITCH09270C2 is a 300-watt, internally matched LDMOS FET, designed for ISM applications with frequencies from 700 to 1000MHz including RF Energy at 915MHz. It Can be used in Class AB/B and Class C configuration, supporting both CW and pulsed signal.

ITCH09270C2



•Typical Performance (On Innogration fixture with device soldered):

VDD = 30 Volts, I_{DQ} = 10 mA, CW signal

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	IDS(A)	Gain(dB)	EFF(%)
910	40.3	54.9	310	15.8	14.6	65.0%
915	40.3	54.9	307	15.5	14.6	66.0%
920	40.3	54.7	300	15.1	14.4	66.0%

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	70	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.27	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=1mA)	V_{DSS}	65	70		V
Zero Gate Voltage Drain Leakage Current	I_{DSS}			10	μA

(V_{DS} = 28 V, V_{GS} = 0 V)					
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 uA)	$V_{GS(th)}$		1.8		V
Gate Quiescent Voltage (V_{DD} = 28 V, I_{DQ} = 2000mA, Measured in Functional Test)	$V_{GS(Q)}$		3		V

Functional Tests (On Innogration demo, 50 ohm system) :V_{DD} = 28 Vdc, I_{DQ} = 10 mA, f = 915MHz, Pulse CW, Pulse Width=20 us, Duty cycle=10% .

Power Gain @P3dB	G_p		14.5		dB
3dB Compression Point	P_{-3dB}		300		W
Drain Efficiency@P3dB	η_D		65		%
Input Return Loss	IRL		-7		dB

Load Mismatch (On Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} =2000mA, f = 915 MHz

VSWR 10:1 at 300W pulse CW Output Power	No Device Degradation

Reference Circuit of Test Fixture Assembly Diagram

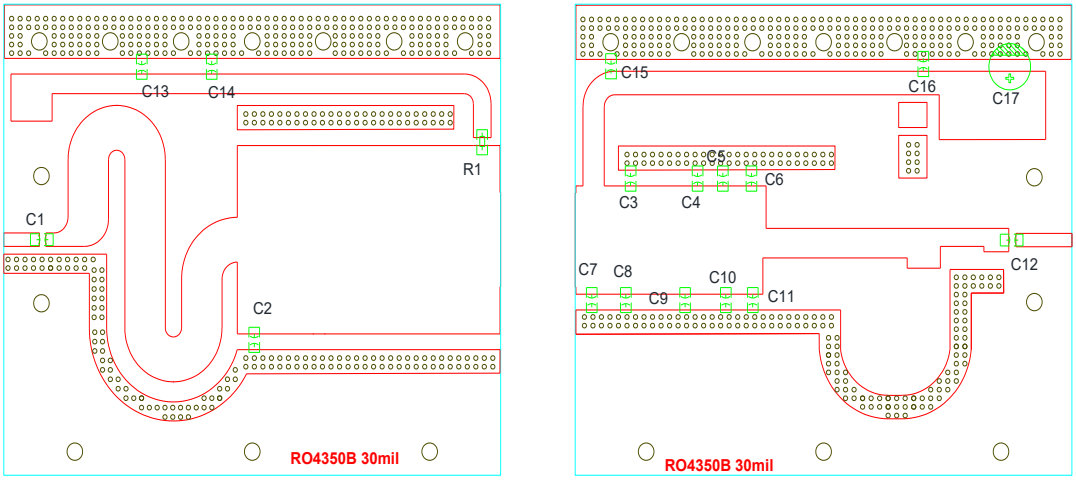
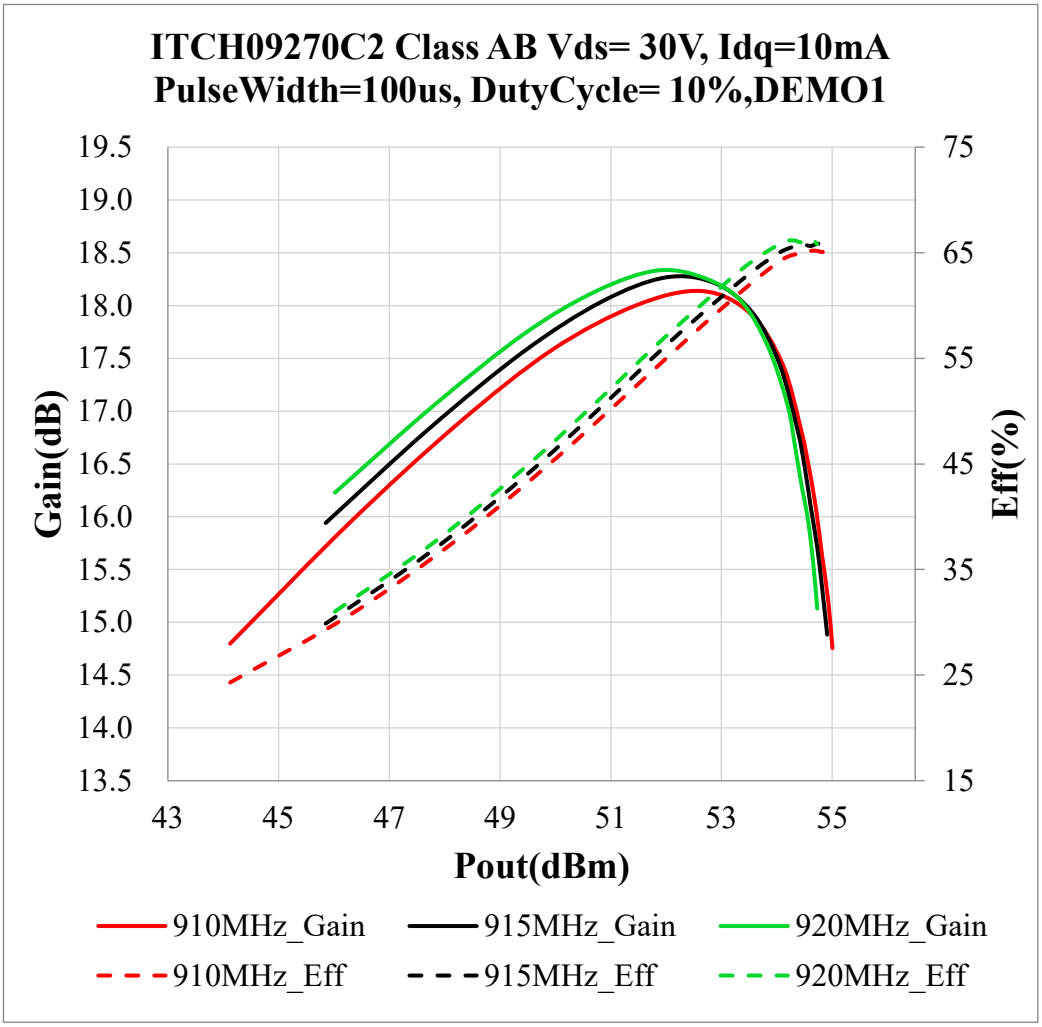


Figure 1. Test Circuit Component Layout

Table 1. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C1, C12, C14, C15	82pF	ATC 800B
C2, C9	3.3pF	ATC 800B
C3, C8	6.8pF	ATC 600F
C4, C6, C10	2.7pF	ATC 600F
C5, C11	1.8pF	ATC 800B
C7	8.2pF	ATC 800B
C13, C16	Ceramic multilayer capacitor, 10uF 50V	
C17	Electrolytic Capacitor ,470uF,63V	
R1	Chip Resistor,9.1Ω， 1206	
PCB	0.762mm [0.030"] thick, εr=3.50, Rogers 4350B, 1 oz. copper	

TYPICAL CHARACTERISTICS

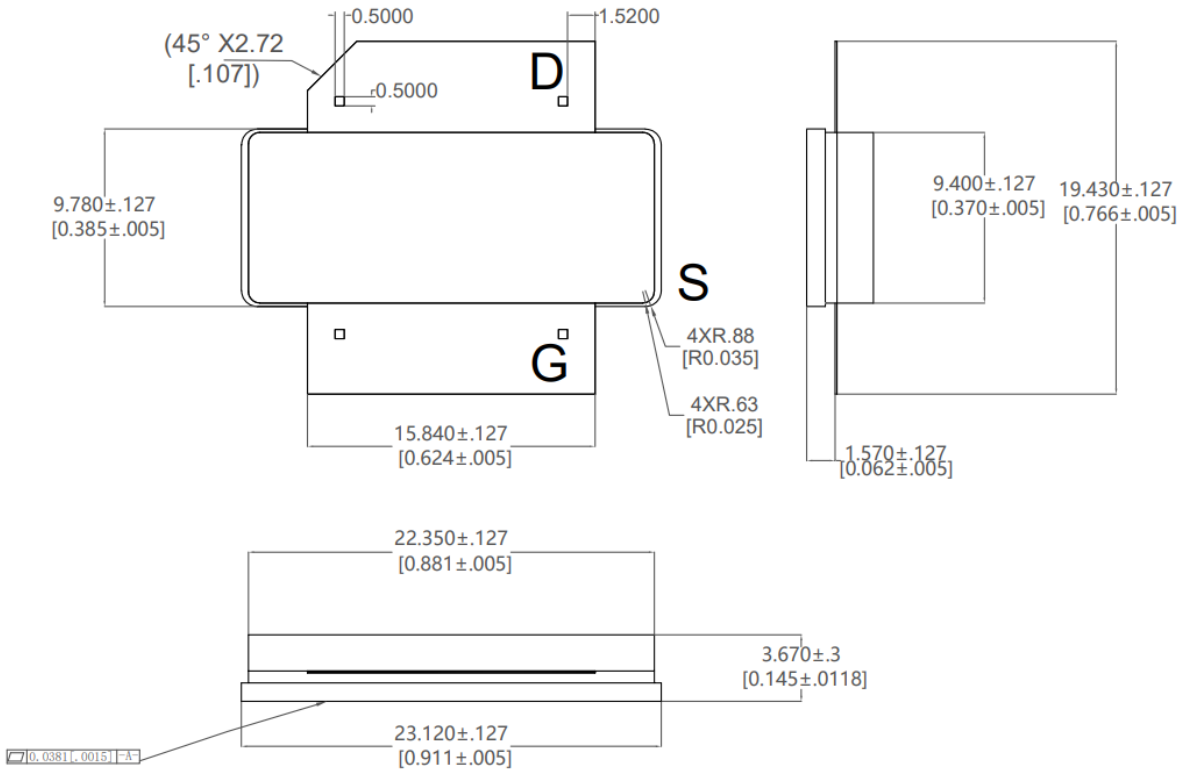


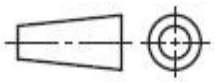
Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
910	54.26	266.7	64.7	17.15	54.94	311.7	65.2
915	54.13	259.0	65.2	17.28	54.83	304.0	65.8
920	54.01	251.9	65.6	17.34	54.69	294.7	66.0

Package Outline

Flangeless ceramic package;

INP-688-2-EL（C2)



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2020/12/2	**Rev 1.0**	**Preliminary Datasheet**

Application data based on TK-20-11

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