

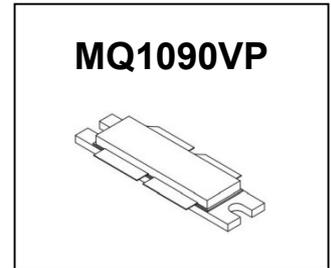
MQ1090VP LDMOS TRANSISTOR

Document Number: MQ1090VP
Preliminary Datasheet V1.1

1000W, UHF 50V High Power RF LDMOS FETs

Description

The MQ1090VP is a 1000-watt capable, high performance, internally matched LDMOS FET, designed for narrow band pulsed amplifier applications within UHF band up to 1GHz



- Typical **pulsed CW** Performance (on innogration narrow band test fixture with device soldered):
Frequency:1000MHz,; Vds = 50 Volts, Idq = 100 mA, TA = 25 C

Pulse condition	Gp (dB)	P _{OUT} (W)	η _D @P _{OUT} (%)
pulse width 100us duty cycle 10%	14.5	1100	57

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	115	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+55	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case,Case Temperature 80°C, 1000W Pout, Pulse width: 100us, duty cycle: 10%, Vds=50 V, IdQ = 100 mA , Frequency at 1000MHz	R _{θJC}	0.02	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Drain-Source Breakdown Voltage (V _{GS} =0V; I _D =100uA)	V _{DSS}	115	---	---	V
Zero Gate Voltage Drain Leakage Current	I _{DSS}	---	---	10	μA

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($V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$)					
Gate--Source Leakage Current ($V_{GS} = 6\text{ V}$, $V_{DS} = 0\text{ V}$)	I_{GSS}	---	---	1	μA
Gate Threshold Voltage ($V_{DS} = 50\text{ V}$, $I_D = 600\text{ uA}$)	$V_{GS(th)}$	---	1.6	---	V
Gate Quiescent Voltage ($V_{DD} = 50\text{ V}$, $I_{DQ} = 100\text{ mA}$, Measured in Functional Test)	$V_{GS(Q)}$		3.0		V

Functional Tests (In Innogration test fixture, 50 ohm system) : $V_{DD} = 50\text{ Vdc}$, $I_{DQ} = 100\text{ mA}$, $f = 1000\text{ MHz}$, Pulse CW Signal Measurements.
(Pulse Width=100 μs , Duty cycle=10%), $P_{in}=46\text{ dBm}$

Power Gain	G_p	---	14	---	dB
Output Power	P_{out}	---	1000	---	W
Drain Efficiency@ P_{out}	η_D	---	56	---	%
Input Return Loss	IRL	---	-7	---	dB

Figure 1: 1000MHz Pulsed CW gain and efficiency as a Function of Output Power
Pulse width 100us and duty cycle 10%

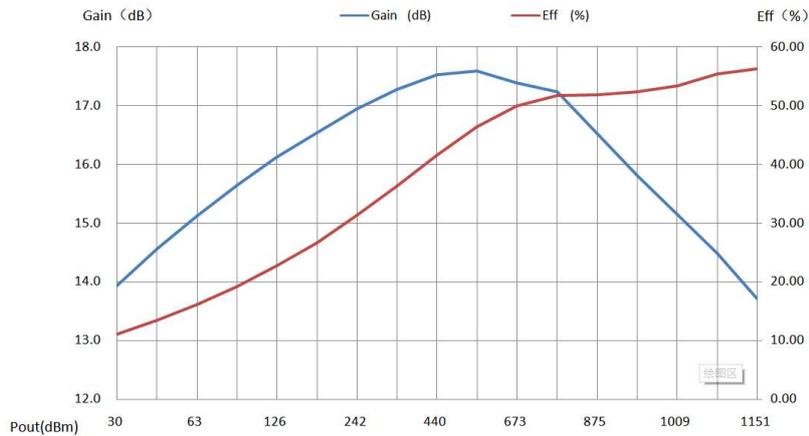
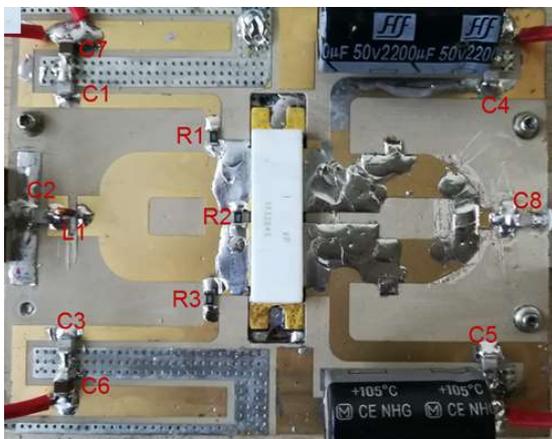


Figure 2: Test fixture photo(1000MHz)



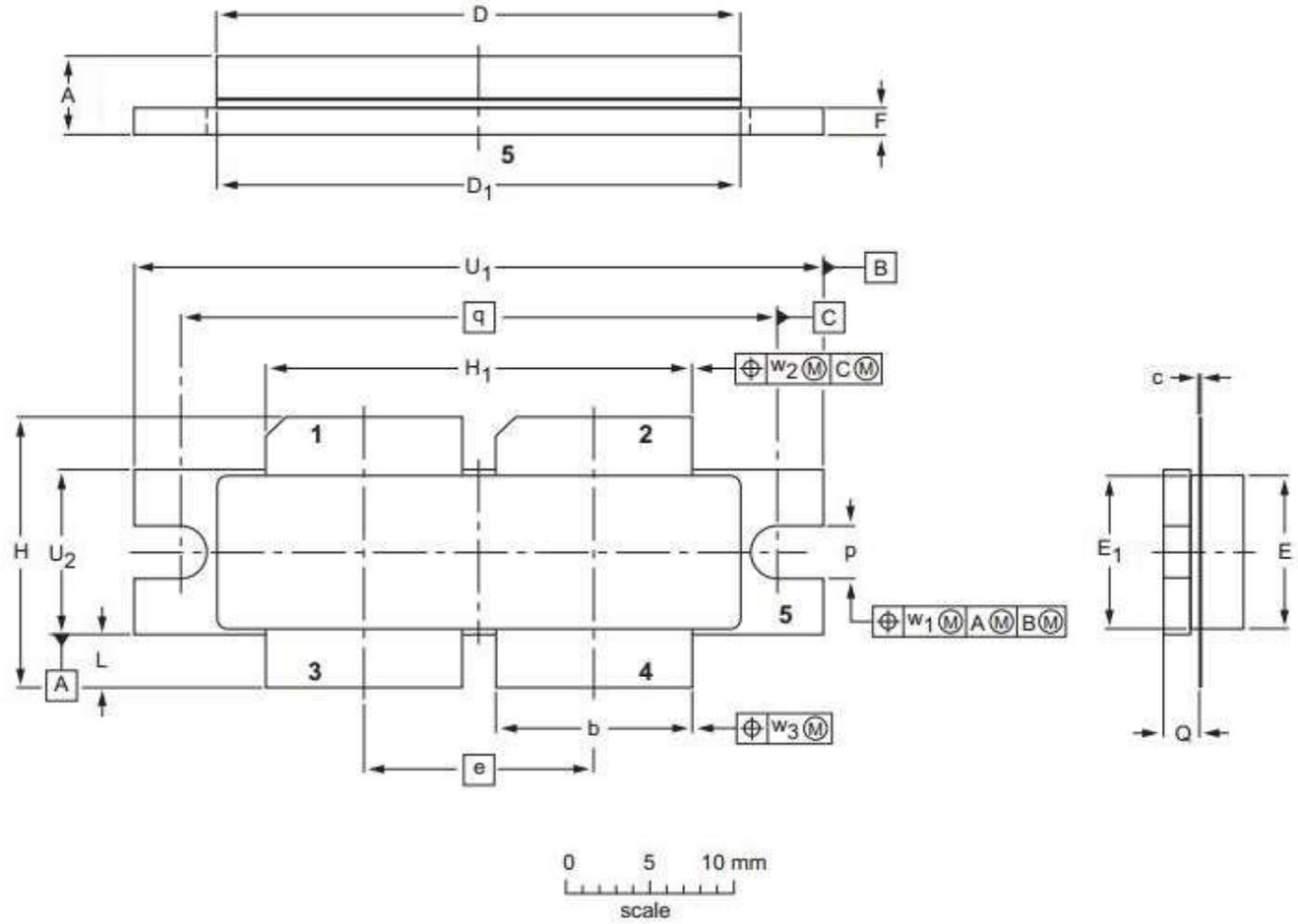
BOM of 1030MHz fixture (PCB 25mil TC600 from Arlon)		
C1,C2,C3,C4,C5,C8	56PF	ATC800B
C6,C7	10UF	
R1,R2,R3	10 Ω	
L1	1turns	Diameter=3mm

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Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	p	Q	q	U ₁	U ₂	W ₁	W ₂	W ₂
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	3.30	2.26	35.56	41.28	10.29	0.25	0.51	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	3.05	2.01		41.02	10.03			
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.130	0.089	1.400	1.625	0.405	0.01	0.02	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.120	0.079		1.615	0.395			

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

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Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2017/11/8	Rev 1.0	Preliminary Datasheet Creation
2022/10/4	Rev 1.1	Modify to 1GHz to be UHF specified product

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