

M2M1502V LDMOS TRANSISTOR

Document Number: M2M1502V
Production Datasheet V1.0

1.5GHz, 20W, 50V High Power RF LDMOS FETs

Description

The M2M1502V is a 20-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies HF to 1.5GHz.

It can support pulsed, CW or any modulated signal in form of linear or saturated operations.



•Typical Performance (On Innogration narrow band fixture with device soldered):

Pulsed CW, 20uS width, 10% dule cycle, Vds=50V, Idq=95mA

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1485.00	44.06	25.47	57.94	19.42	44.69	29.45	58.62
1500.00	43.69	23.38	57.36	19.51	44.44	27.77	58.44
1515.00	43.39	21.82	56.77	19.47	44.22	26.43	58.72

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 30-512MHz (Jammer, Ground/Air communication)
- 4G/5G cellular base station
- 470-860MHz (TV UHF)
- Avionics 960-1215MHz
- L band 1200-1400MHz

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c= 85^{\circ}C, T_j=200^{\circ}C, DC$ test	$R_{\theta JC}$	1.8	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

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Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

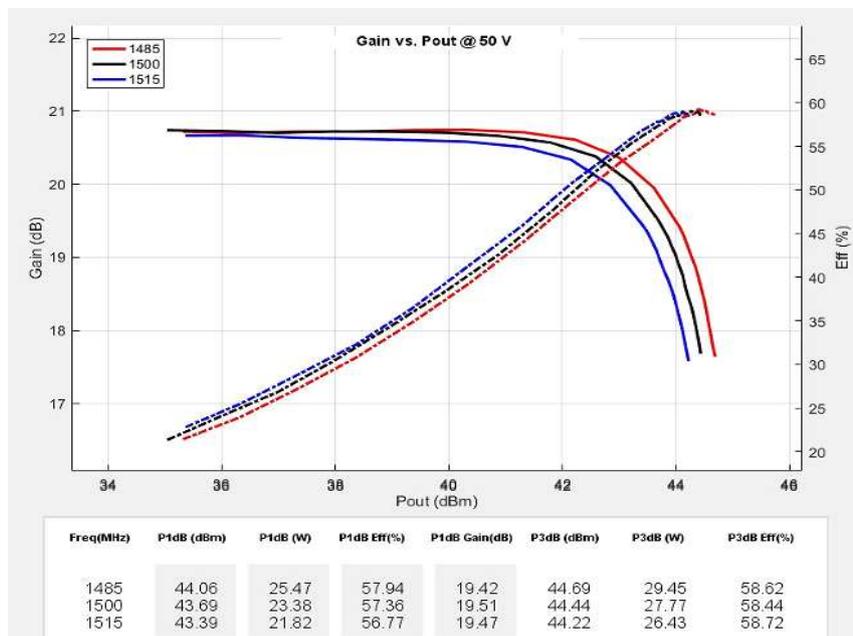
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage $V_{GS}=0, I_{DS}=1.0mA$	$V_{(BR)DSS}$		115		V
Zero Gate Voltage Drain Leakage Current $(V_{DS} = 50V, V_{GS} = 0 V)$	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current $(V_{GS} = 10 V, V_{DS} = 0 V)$	I_{GSS}	—	—	1	μA
Gate Threshold Voltage $(V_{DS} = 50V, I_D = 600 \mu A)$	$V_{GS(th)}$	—	2.73	—	V
Gate Quiescent Voltage $(V_{DD} = 50 V, I_D = 95 mA, \text{Measured in Functional Test})$	$V_{GS(Q)}$	—	3.16	—	V
Common Source Input Capacitance $(V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)$	C_{ISS}		24		pF
Common Source Output Capacitance $(V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)$	C_{OSS}		10		pF
Common Source Feedback Capacitance $(V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)$	C_{RSS}		0.1		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) $V_{DD} = 50 Vdc, I_{DQ} = 95mA, f = 1.5GHz, \text{Pulsed CW Signal, pin}=23dBm$

Power Gain@Pout	G_p	—	20	—	dB
Output Power	P_{out}		20	25	W
Drain Efficiency@Pout	η_D		55	—	%
Input Return Loss	IRL	—	-5	—	dB

TYPICAL CHARACTERISTICS

Figure 1: Pulsed CW Gain and Power Efficiency as a Function of Pout at 1.5GHz



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Figure 2: Network analyzer output S11/S21

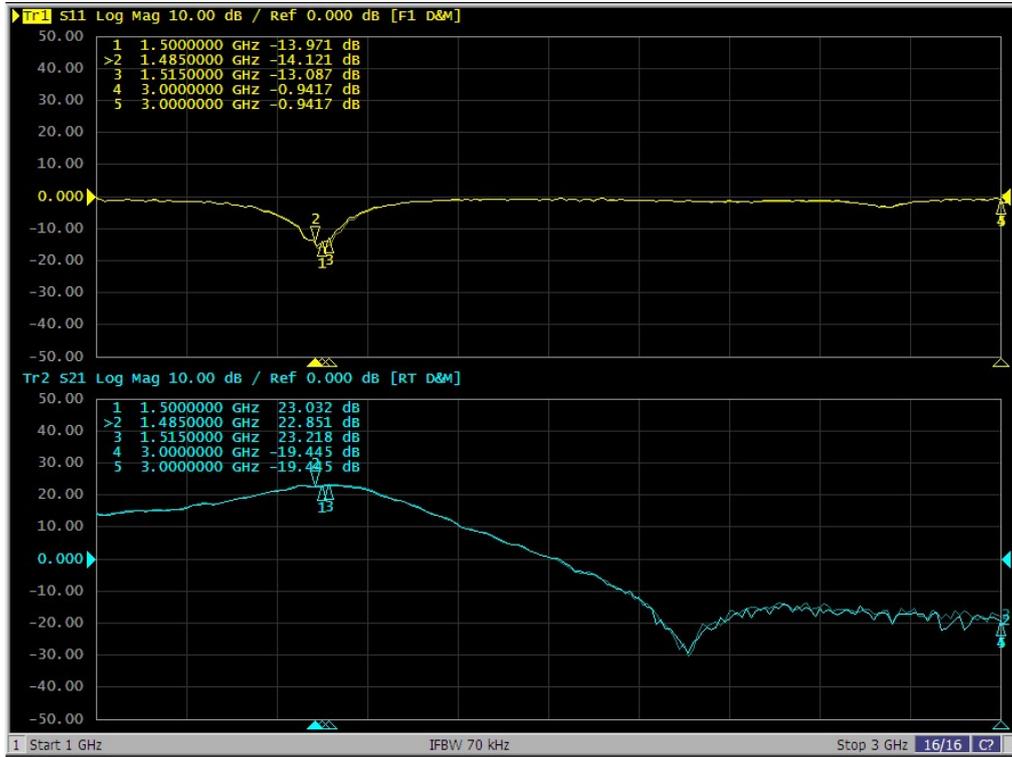
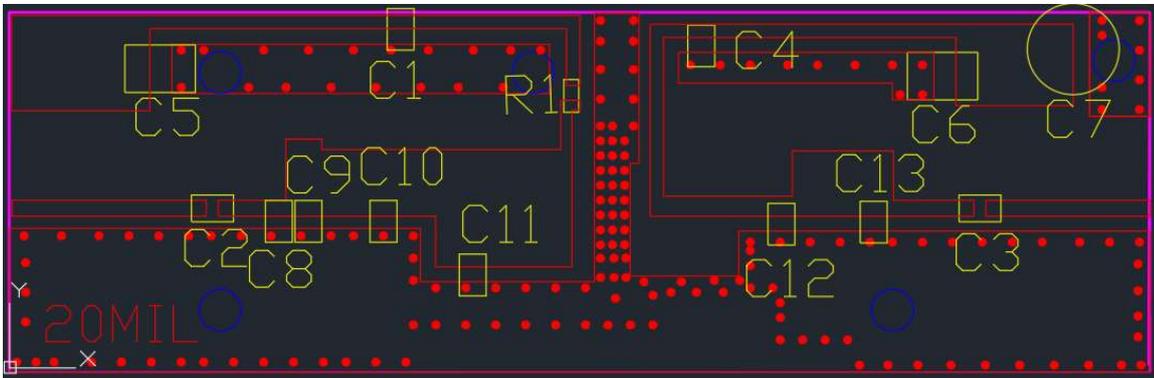


Figure 3. Test Circuit Component Layout (PCB Roger 4350B 20Mil, PCB file upon request)



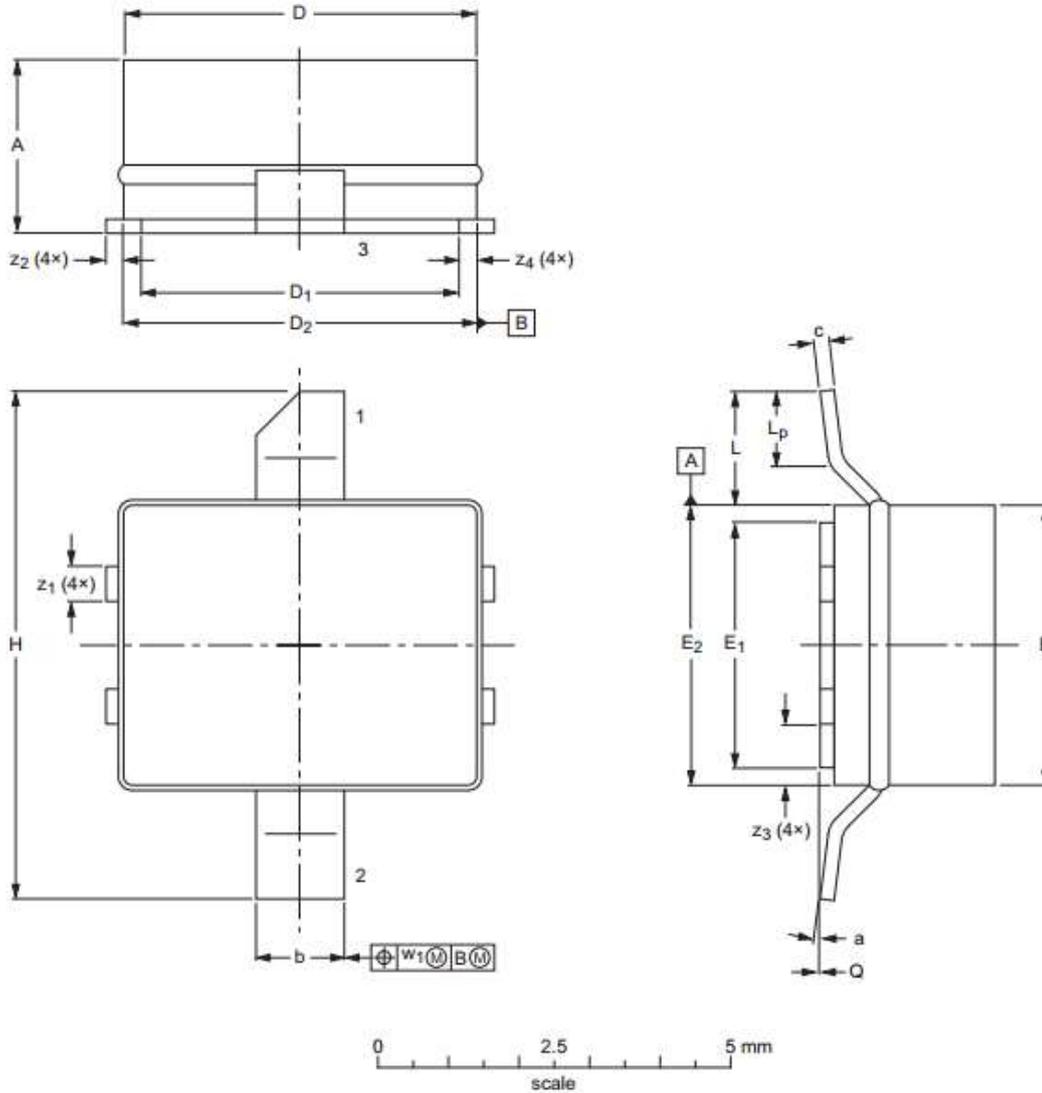
BOM		
C1,C2,C3,C4	39pF	0805
R1	10 ohm	0603
C7	470 uF/63V	
C8	0.2pF	0805
C9	0.6pF	0805
C10	1.5pF	0603
C11	6.8pF	0603
C12	1.2pF	0603
C13	2pF	0603
C5,C6	10 uF	1210

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Package Outline

Earless Flanged ceramic package; 2 leads(1-Drain,2-Gate,3-Source)



UNIT	A	b	c	D	D ₁	E	E ₁	E ₂	H	L	L _p	Q	w ₁	z ₁	z ₂	z ₃	z ₄	α
mm	2.34	1.35	0.23	5.16	4.65	4.14	3.63	4.14	7.49	2.03	1.02	0.1	0.25	0.58	0.25	0.97	0.51	7°
	2.13	1.19	0.18	5.00	4.50	3.99	3.48	3.99	7.24	1.27	0.51	0.0		0.43	0.18	0.81	0.00	0°

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-MM					18/6/2014

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2022/12/15	V1.0	Production Datasheet Creation

Application data based on ZXY-22-42

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