

M2U1010V LDMOS TRANSISTOR

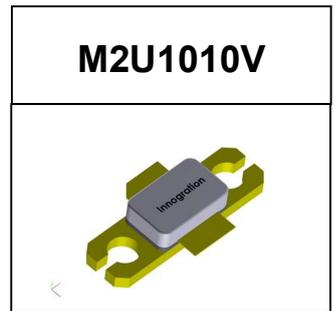
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Preliminary Datasheet V1.0

1000MHz, 100W, 50V High Power RF LDMOS FETs

Description

The M2U1010V is a 100-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies HF to 1.0 GHz.

It can support pulsed, CW or any modulated signal in form of linear or saturated operations.



- Typical Performance (On Innegration narrow band fixture with device soldered): Pulsed CW, 20uS width, 10% dule cycle

Vds= 50V, IDQ =100mA(Vgs =3.16V)							
Freq (MHz)	P1dB(dBm)	P1dB(W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB(dBm)	P3dB(W)	P3dB Eff(%)
915	49.69	93.1	64.96	22.6	50.35	108.36	65.43

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c= 85^\circ\text{C}$, $T_j=200^\circ\text{C}$, DC test	$R_{\theta JC}$	1.1	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

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Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

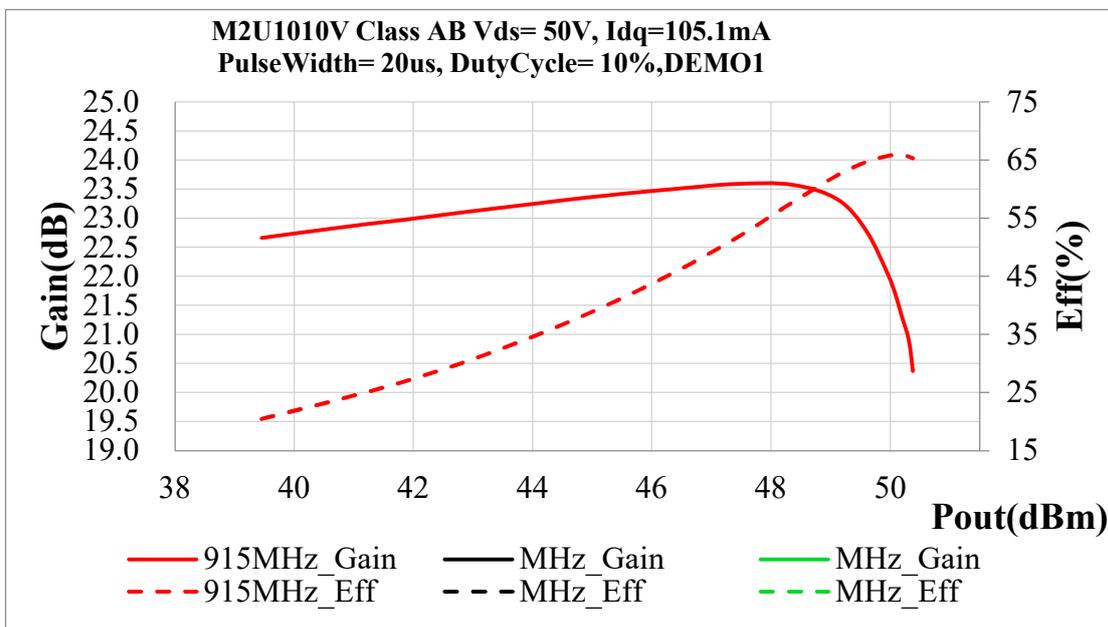
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage $V_{GS}=0, I_{DS}=1.0mA$	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current $(V_{DS} = 50V, V_{GS} = 0 V)$	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current $(V_{GS} = 10 V, V_{DS} = 0 V)$	I_{GSS}	—	—	1	μA
Gate Threshold Voltage $(V_{DS} = 50V, I_D = 600 \mu A)$	$V_{GS(th)}$	—	2.73	—	V
Gate Quiescent Voltage $(V_{DD} = 50 V, I_D = 100 mA, \text{Measured in Functional Test})$	$V_{GS(Q)}$	—	3.16	—	V
Common Source Input Capacitance $(V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)$	C_{ISS}		85		pF
Common Source Output Capacitance $(V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)$	C_{OSS}		36		pF
Common Source Feedback Capacitance $(V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)$	C_{RSS}		1.2		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) $V_{DD} = 50 Vdc, I_{DQ} = 100mA, f = 915 MHz, CW$ Signal Measurements, $P_{in}=27dBm$

Power Gain@Pout	G_p	—	22	—	dB
Output Power	P_{out}		100		W
Drain Efficiency@Pout	η_D	—	60	—	%
Input Return Loss	IRL	—	-5	—	dB

TYPICAL CHARACTERISTICS

Figure 1: Pulsed CW Gain and Power Efficiency as a Function of Pout at 915MHz



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Figure 2: Network analyzer output S11/S21

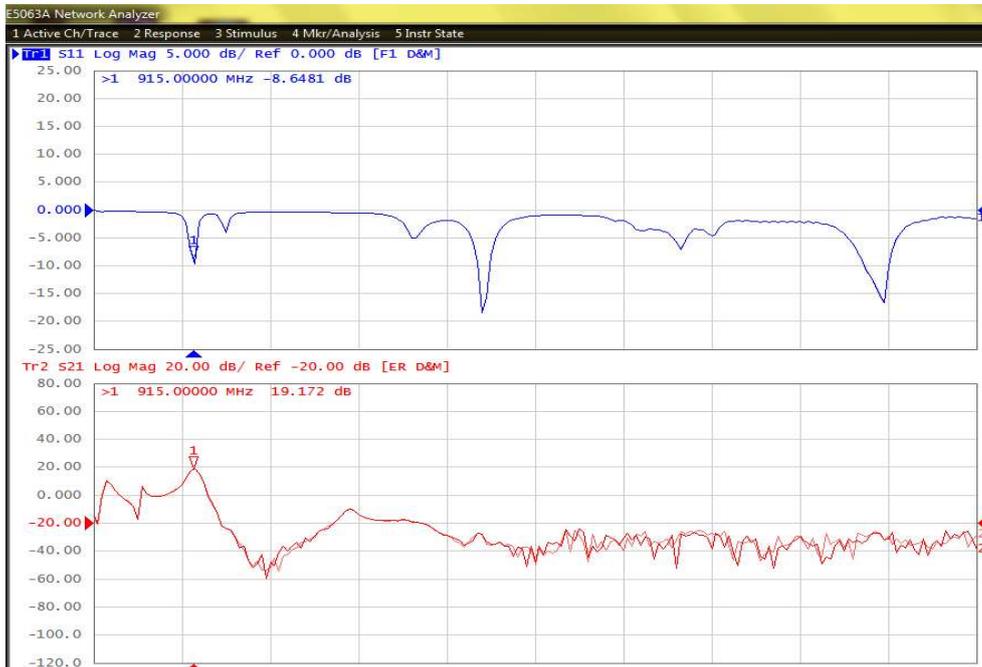
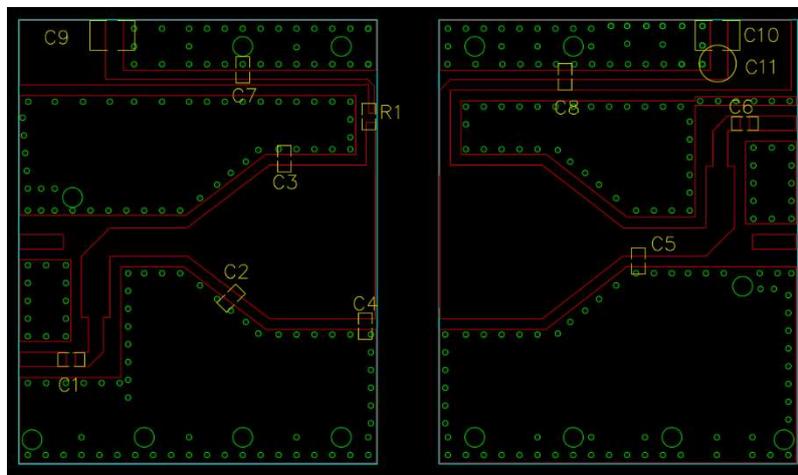


Figure 3. Test Circuit Component Layout
(PCB Roger 4350B 30Mil, PCB file upon request)



Component	Value	Quantity
U1	M2U1010V	1
C1、C6、C7、C8	33pF	4
C3、C4	15pF	2
C2	10pF	1
C5	12pF	1
C11	470uF/63V	1
C9、C10	10uF	2
R1	10Ω	1

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Package Outline

Flanged ceramic package; 2 leads

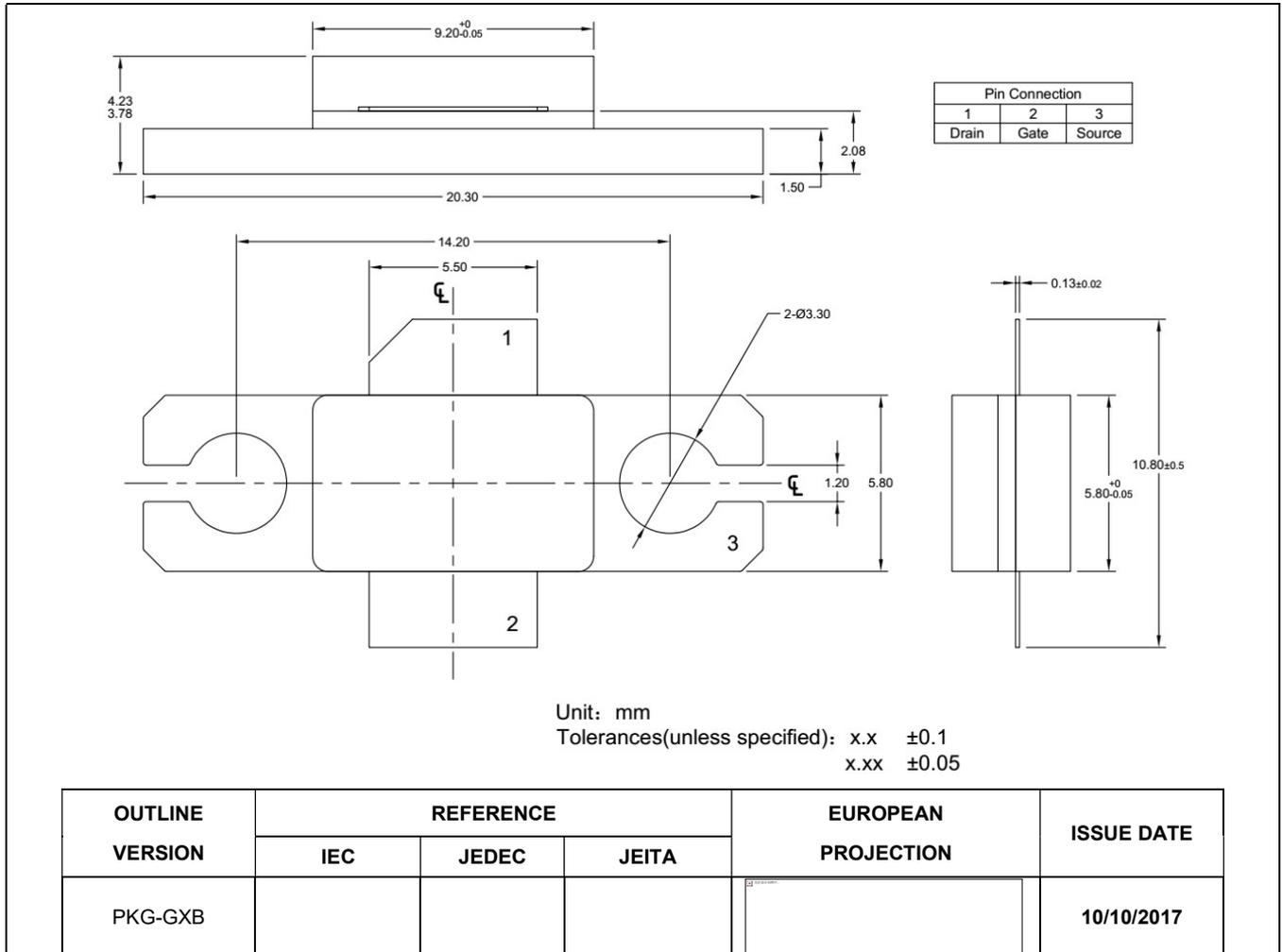


Figure 1. Package Outline PKG-G2E

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2022/12/5	V1.0	Preliminary Datasheet Creation

Application data based on ZYX-22

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