



500W,50V RF LDMOS Transistor

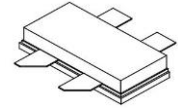
ITEV10500B4

Description

The ITEV10500B4 is a 500watt capable, Doherty paired LDMOS transistor, ideal for 4G/5G cellular applications from 0.6 to 1GHz..

It can be configured as asymmetrical Doherty delivering 80W average power, according to normal 8dB back off.

There is no guarantee of performance when this part is used outside of stated frequencies.



- Typical Doherty RF Performance (On Innegration fixture with device soldered).

Vds=50V Idq_main=460mA, Vgs_peak=1.8V

Freq (MHz)	Pulse CW Signal			P _{avg} =49dBm WCDMA Signal		
	Gain P1dB (dB)	P3dB (W)	Eff@P3dB (%)	Gp (dB)	Eff(%)	ACPR _{5M} (dBc)
869	18.32	528.3	56.5	19	48.1	-28.7
881	18.28	538.7	58.3	19	48.2	-30.3
894	18.05	516.2	59.2	19	48.5	-32.6

- Typical Doherty RF Performance (On Innegration fixture with device soldered).

Vds=50V Idq_main=330mA, Vgs_peak=1.8V

Freq (MHz)	Pulse CW Signal			P _{avg} =49dBm WCDMA Signal		
	Gain P1dB (dB)	P3dB (W)	Eff@P3dB (%)	Gp (dB)	Eff(%)	ACPR _{5M} (dBc)
758	16.71	546.0	61.3	17.2	48.1	-28.2
780	16.51	512.4	62.7	17.2	50.7	-30.0
803	16.76	514.9	58.2	17.3	51.6	-33.6

Applications

- Asymmetrical Doherty amplifier within 0.6-1GHz
- UHF TV
- P band power amplifier

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

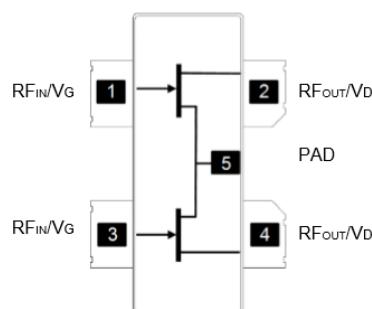




Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c = 85^{\circ}\text{C}$, $T_j = 200^{\circ}\text{C}$, DC test	$R_{\theta JC}$	0.4	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Drain-Source Voltage $V_{GS}=0$, $I_{DS}=100\mu\text{A}$	$V_{(BR)DS}$		110		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 90\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 11\text{V}$, $V_{DS} = 0\text{V}$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 50\text{V}$, $I_D = 600\mu\text{A}$)	$V_{GS(th)}$	—	2	—	V
Gate Quiescent Voltage ($V_{DD} = 50\text{V}$, $I_D = 500\text{mA}$, Measured in Functional Test)	$V_{GS(Q)}$	—	3.3	—	V

Load Mismatch (In Innogrations Test Fixture, 50 ohm system): $V_{DD} = 50\text{Vdc}$, $I_{DQ} = 500\text{mA}$, $f = 894\text{MHz}$

VSWR 10:1 at 80W WCDMA Output Power	No Device Degradation
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869-894MHz application board

Reference Circuit of Test Fixture Assembly Diagram 20mils RO4350B

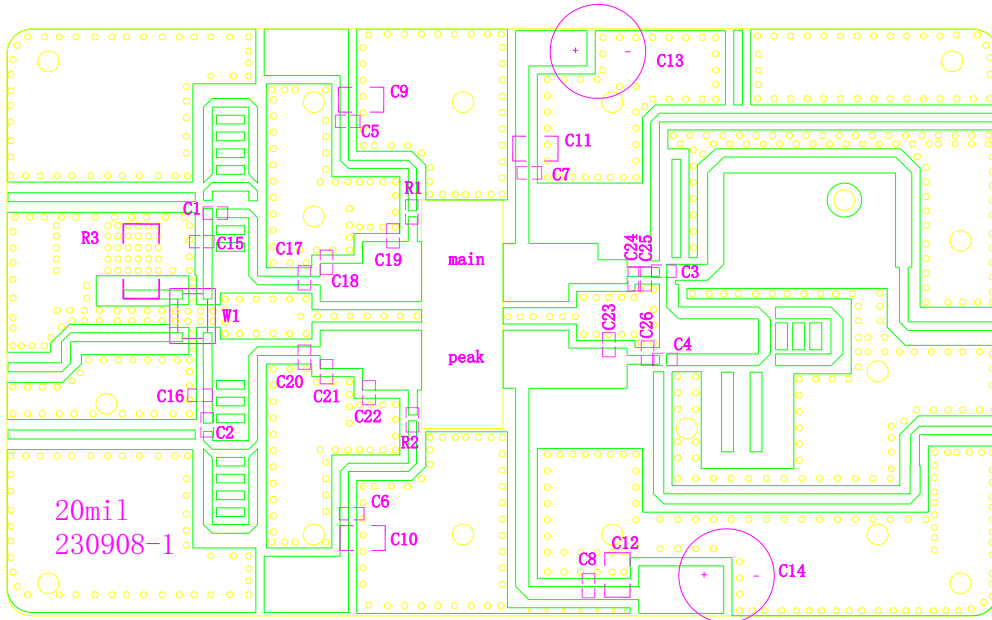


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Designator	Footprint	Comment	Quantity
C1, C2, C25, C26	0603	10 pF	4
C3, C17, C18, C19, C20, C21, C22, C23	0603	6.8 pF	8
C4, C5, C6, C7, C8	0603	68 pF	5
C9, C10, C11, C12	1210	10uF/100V	4
C13, C14		220uF/63V	2
C15	0603	2.7 pF	1
C16	0603	1.1 pF	1
C24	0603	2 pF	1
R1, R2	0603	10R	2
R3	2512	RFR50N-20CT0410B	1
W1		DC07F02 (YANTEL 2dB)	1

(pF capacitors are ATC 600S series)

TYPICAL CHARACTERISTICS

Figure 5. Power Gain and Drain Efficiency as function of Power Output at $I_{dq}=460\text{mA}$

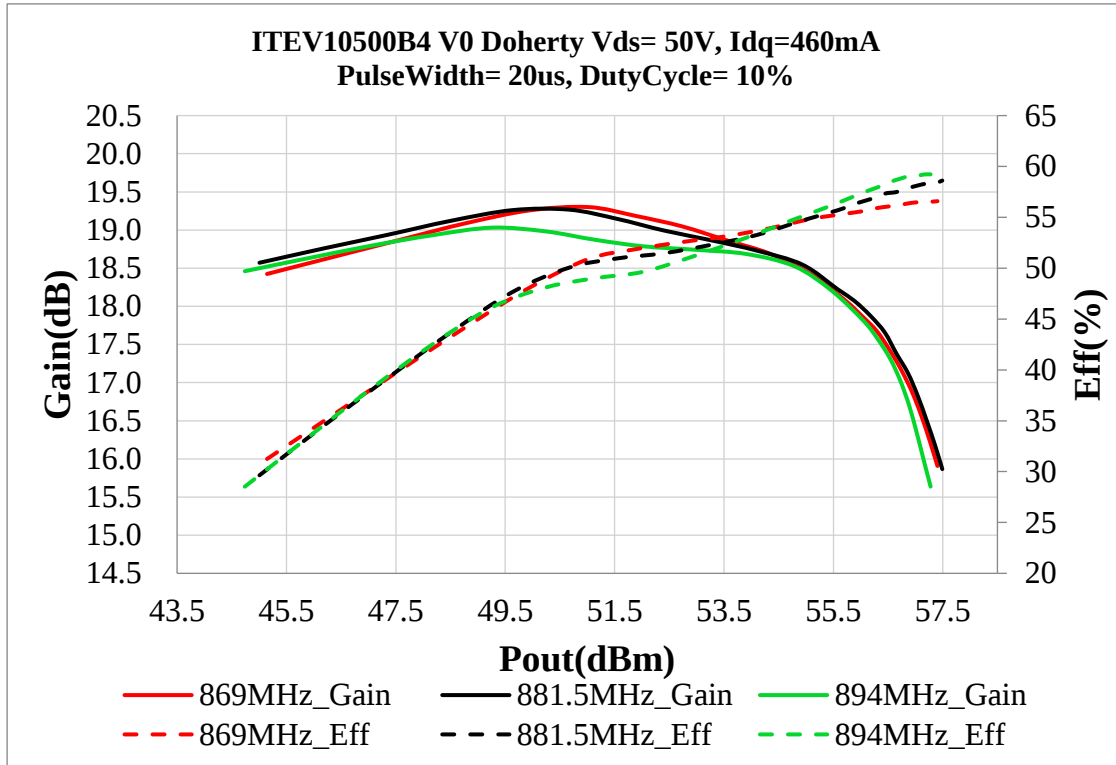


Figure 5. Network analyzer output S11/S21



758-803MHz application board

Reference Circuit of Test Fixture Assembly Diagram 20mils RO4350B

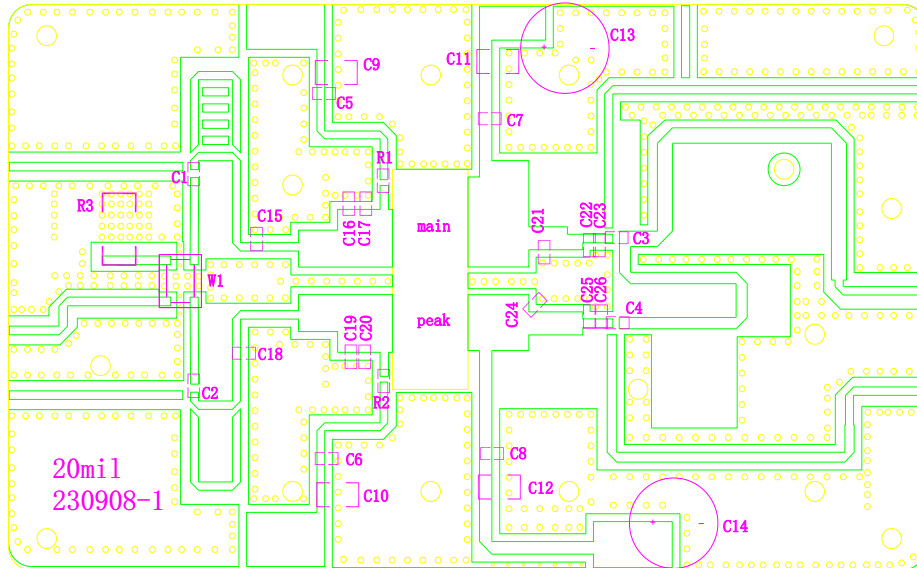


Figure 6. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Designator	Footprint	Comment	Quantity
C1, C2, C15, C16, C21, C24	0603/0805	10 pF	6
C3, C16, C17, C19, C20	0603/0805	15 pF	5
C4, C5, C6, C7, C8	0603/0805	47 pF	5
C9, C10, C11, C12	1210	10uF/100V	4
C13, C14		470uF/63V	2
C22, C23, C25, C26	0603/0805	6.8 pF	4
R1, R2	0603/0805	10Ω	2
R3	2512	51 Ω	1
W1		DC07F02 (YANTEL 2dB)	1

(pF capacitors are ATC 600S series)

TYPICAL CHARACTERISTICS

Figure 7. Power Gain and Drain Efficiency as function of Power Output at $I_{dq}=330\text{mA}$

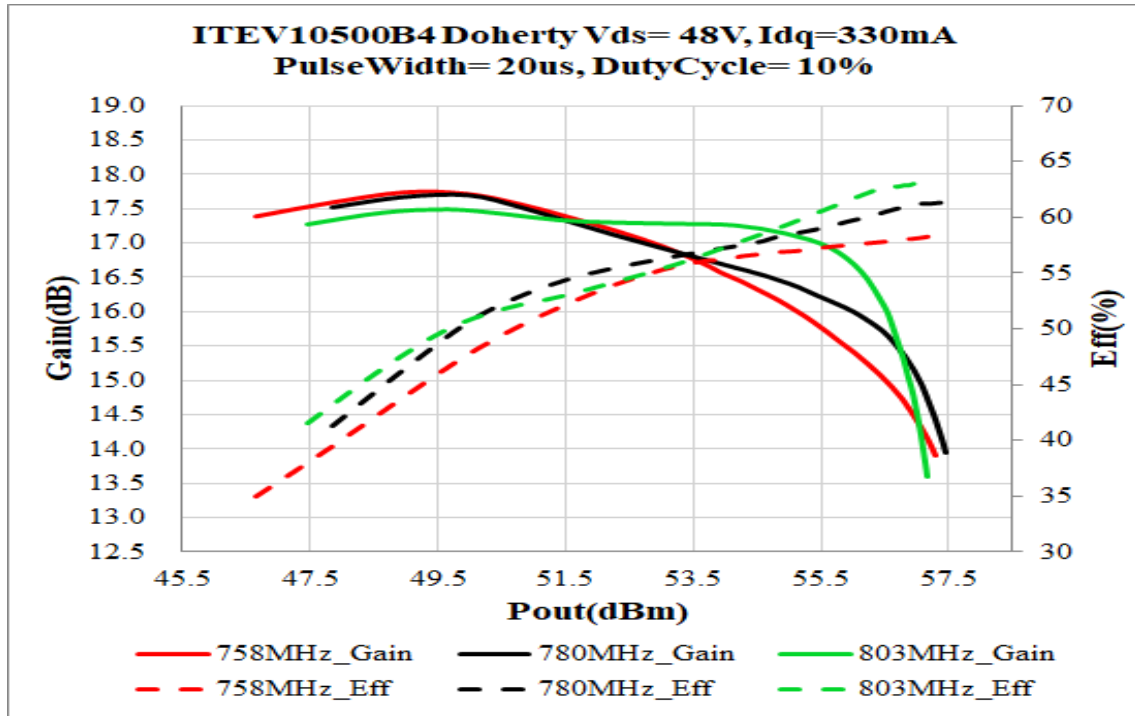
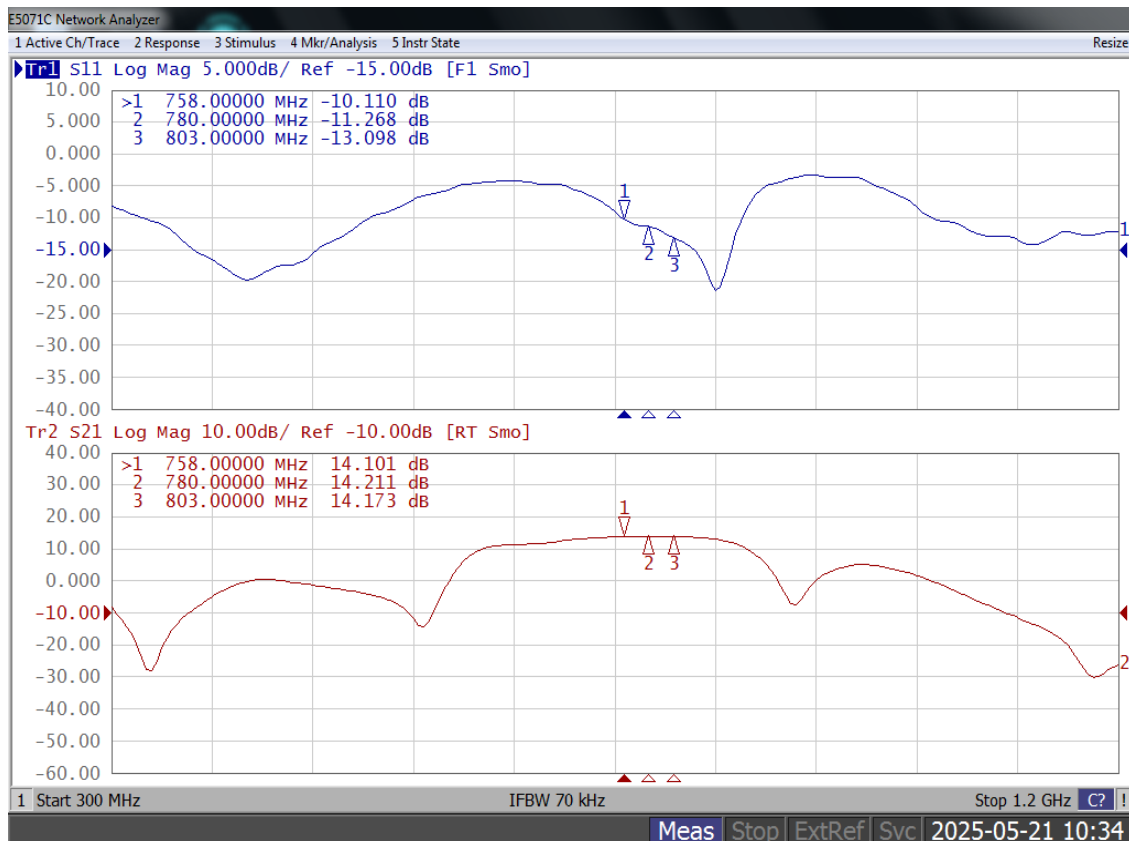
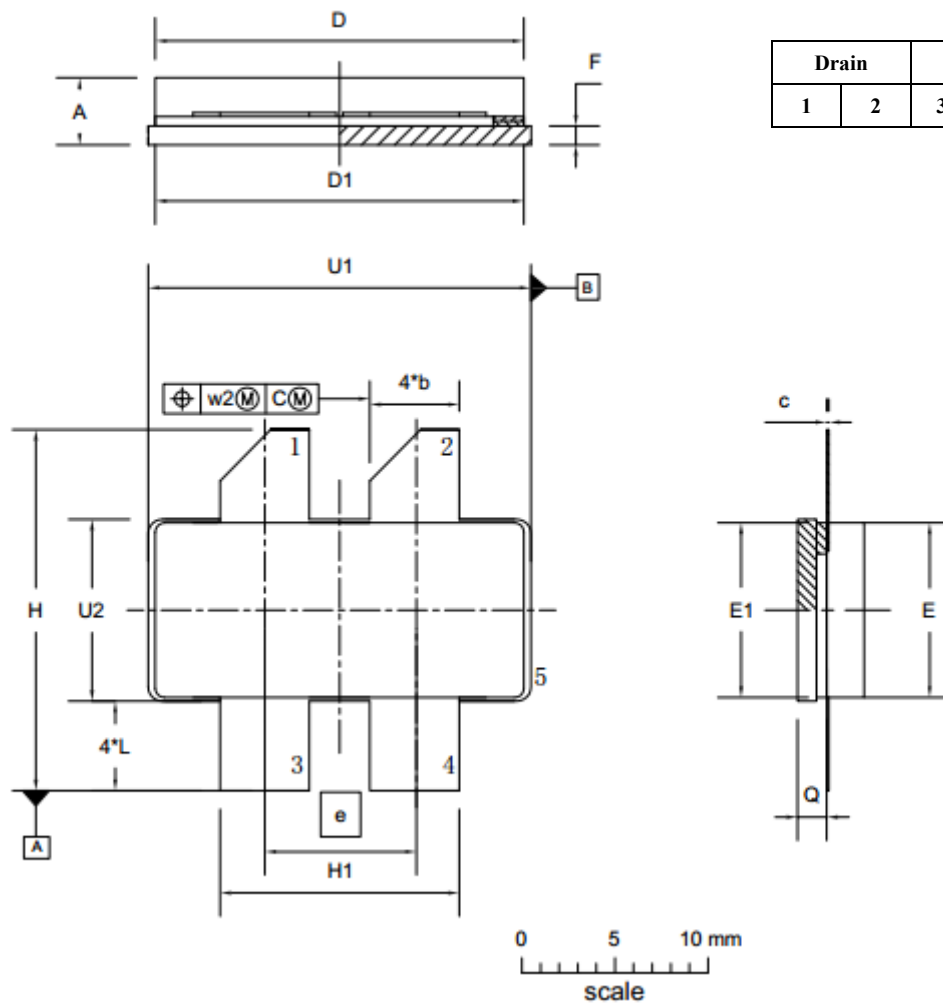


Figure 8. Network analyzer output S11/S21





Earless Flanged Ceramic Package; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₁	W ₂
mm	4.72	4.67	0.15	20.02	19.96	7.90	9.50	9.53	1.14	19.94	12.98	5.33	1.70	20.70	9.91	0.25	0.51
	3.43	4.93	0.08	19.61	19.66		9.30	9.25	0.89	18.92	12.73	4.32	1.45	20.45	9.65		
inches	0.186	0.194	0.006	0.788	0.786	0.311	0.374	0.375	0.045	0.785	0.511	0.210	0.067	0.815	0.390	0.01	0.02
	0.135	0.184	0.003	0.772	0.774		0.366	0.364	0.035	0.745	0.501	0.170	0.057	0.805	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013



Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2023/10/20	Rev 1.0	Preliminary Datasheet
2025/5/22	Rev 1.1	Add 758-803MHz application data

Application data based on LSM-23-32/25-12

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