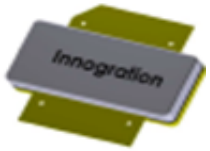
STCV13700RC2 LDMOS TRANSISTOR

Document Number: STCV13700RC2
Preliminary Datasheet V1.0

700W ,50V L band CW RF Power Transistor

STCV13700RC2



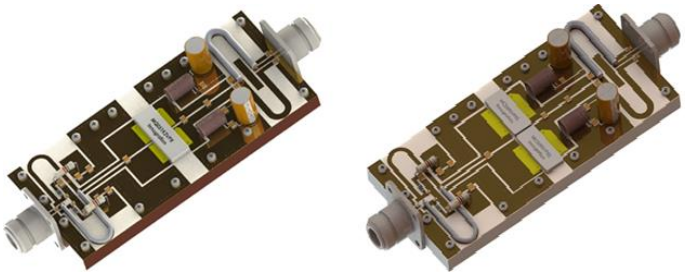
Description

The STCV13700RC2 itself is a 700-watt capable, high performance, internal match，single ended GaN HEMT transistor，idea for RF Energy and ISM application at fixed frequency point or very narrow band within 0.9 to 1.3GHz, typically for 915MHz RF heating or 1.3G particle accelerator applications.

There is no guarantee of performance when this part is used outside of stated frequencies.

It is recommended to use paired STCV13700RC2 to enable >1200W designed for ISM application. Compared to similar power level but in single dual-path packaged device, it offers better thermal management and easier maintenance.

Demonstration of paired STCV13700RC2(right) Vs single dual-path device(left) at 915MHz



- Typical performance(on 1.3GHz narrow band application board with **2×STCV13700RC2** devices soldered)

V_{DS}=50V,Vgs=-4.5V, CW,

Freq(MHz)	P_{out}(W)	Pin(dBm)	Gain(dB)	η(%)
1300	1300	46.5	15	75

Applications

- 1.3GHz particle linear accelerator
- L band power amplifier
- Avionics application
- 915MHz RF heating

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	100	mA
Storage Temperature Range	Tstg	-65 to +150	°C

Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 25°C, at Pd=400W **in Paired configurations**	$R_{\theta JC}$	0.32	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=100mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 100mA	$V_{GS(th)}$	-4	-	-2	V
Gate Quiescent Voltage	VDS =50V, IDS=200mA, Measured in Functional Test	$V_{GS(Q)}$		--3.2		V

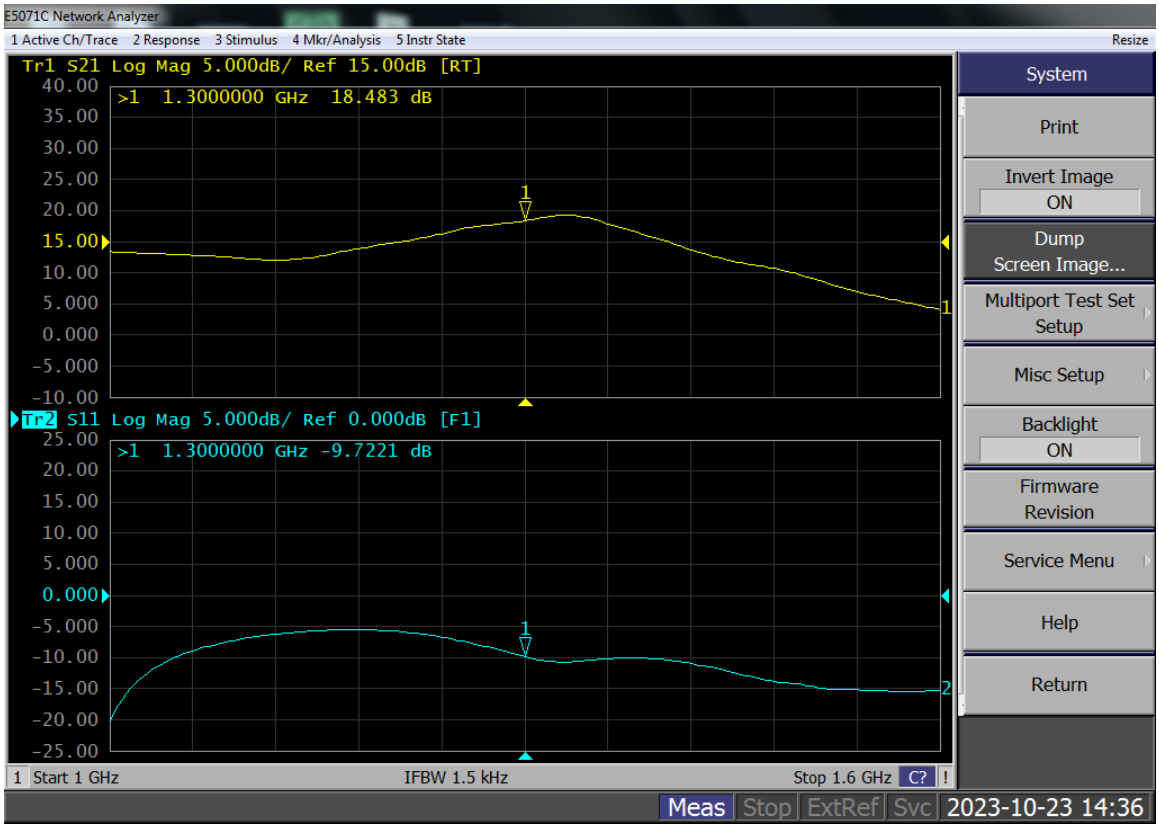
Ruggedness Characteristics in Paired configurations

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	1.3GHz, Pout=1300W pulse CW All phase, No device damages	VSWR		5:1		

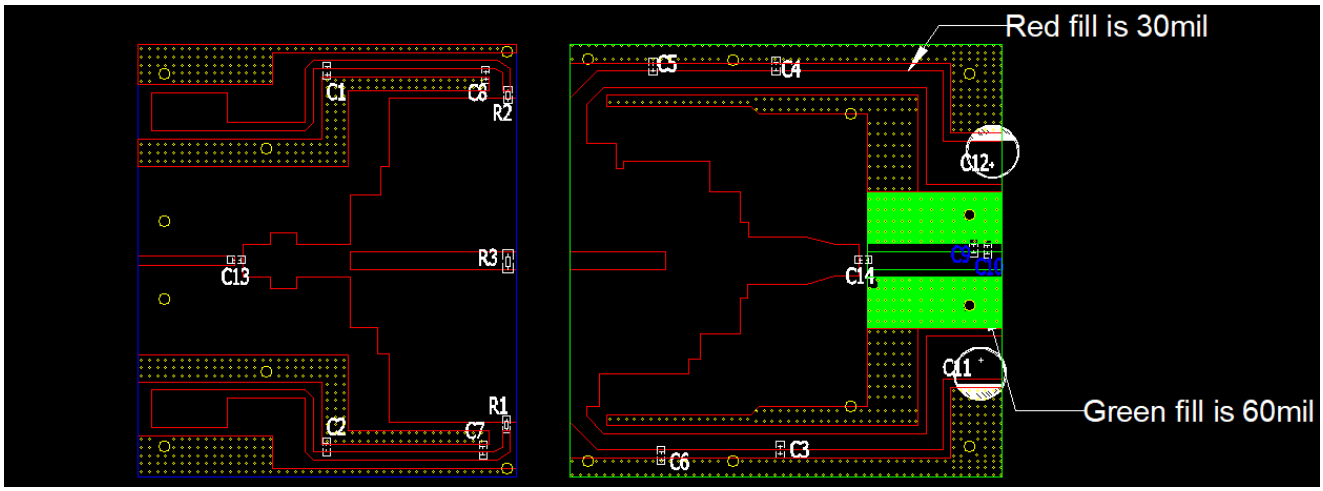
TYPICAL CHARACTERISTICS

STCV13700RC2*2 at 1300MHz

Figure 1: Network analyzer output S11/S21 Vds=50V, Idq=600mA，Pin=0dBm



Reference Circuit of Test Fixture

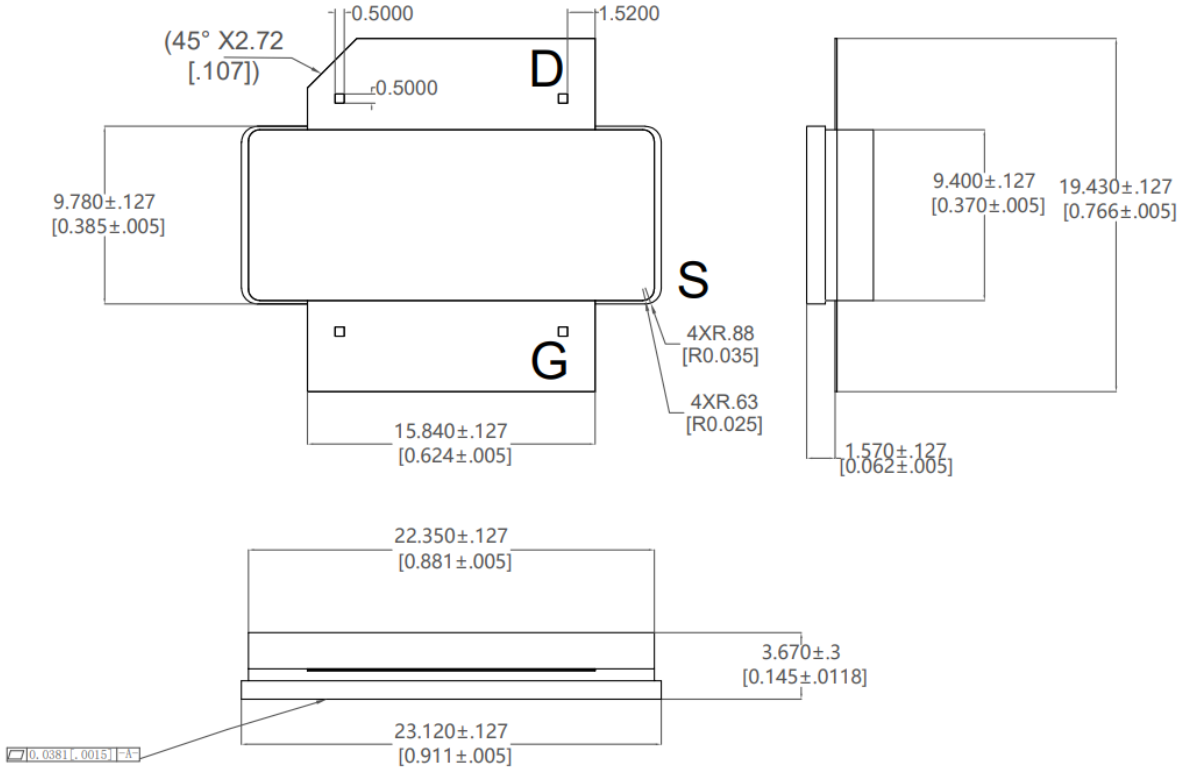


Component	Description	Suggestion
C1~C4	10uF	10uF/100V
C5~C8	68pF	MQ101111
C13	39pF	MQ101111
C14	39pF	MCM-1-300V-D-390J
C11,C12	4700uF/63V	Electrolytic Capacitor
C9	2.2pF	MQ102525
C10	0.5pF	MQ101111
R1,R2	100 Ω	Chip Resistor
R3	10	Chip Resistor
PCB	(Red fill) 30mil Rogers4350	
	(green fill) Taconic RF-35TC-0600-A,thickness 60 mils,1oz copper	

Package Outline

Flangeless ceramic package;

INP-688-2-EL（C2)



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/10/23	Rev 1.0	Preliminary datasheet

Application data based on TC-23-68

Disclaimers