



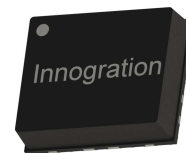
130W,50V Plastic RF LDMOS Transistor

ITGV10130C9

Description

The ITGV10130C9 is a dual path 130-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies up to 1GHz, in 12*10mm QFN plastic package, supporting surface mounted on PCB through high density grounding vias.

It can be configured as Doherty to be as high efficiency and low cost driver for 4G/5G application within 0.6-1GHz.



- Typical Doherty RF Performance (On Innegration fixture with device soldered).

$V_{ds}=50V$, $I_{dq}=100mA$ ($V_m=3.3V$, $V_p=1.6V$)

Freq (MHz)	Pout (dBm)	CCDF (dB)	Ppeak (dBm)	Ppeak (W)	ACPR (dBc)	Gain (dB)	Eff (%)
869	42.50	8.44	50.93	123.9	-27.4	18.8	51.3
881.5	42.50	8.83	51.33	135.9	-28.9	18.4	52.7
894	42.50	8.98	51.48	140.5	-30.8	17.9	52.4

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- P band power amplifier
- All 4G/5G cellular application within 0.6 to 1GHz

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c=85^{\circ}C$, $T_j=200^{\circ}C$, DC test	$R_{\theta JC}$	0.7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2



Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

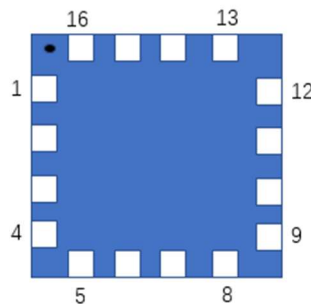
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage $V_{GS}=0$, $I_{DS}=100\mu A$	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 90V$, $V_{GS} = 0V$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 11V$, $V_{DS} = 0V$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 50V$, $I_D = 600\mu A$)	$V_{GS(th)}$	—	2	—	V
Gate Quiescent Voltage ($V_{DD} = 50V$, $I_D = 100mA$, Measured in Functional Test)	$V_{GS(Q)}$	—	3.3	—	V

Load Mismatch (In Innegration Test Fixture, 50 ohm system): $V_{DD} = 50Vdc$, $I_{DQ} = 100mA$, $f = 880MHz$

VSWR 10:1 at 130W pulse CW Output Power	No Device Degradation
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Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)



Pin No.	Symbol	Description
1,2	RF IN/Vgs of Main	RF Input/Gate bias of main path
3,4	RF IN/Vgs of Peak	RF Input/Gate bias of peak path
9,10	RF OUT/Vds of Peak	RF Output/Drain bias of peak path
11,12	RF OUT/Vds of Main	RF Output/Drain bias of main path
Other Pins	GND	Grounding
Package Base	GND	DC/RF Ground. Proposed to be soldered to heatsink plane directly for the best CW thermal and RF performance. Soldered through vias or copper coin allowed for pulsed CW and back off applications, but will result in higher junction temperatures

869-894MHz application board

Reference Circuit of Test Fixture Assembly Diagram

20mils RO4350B

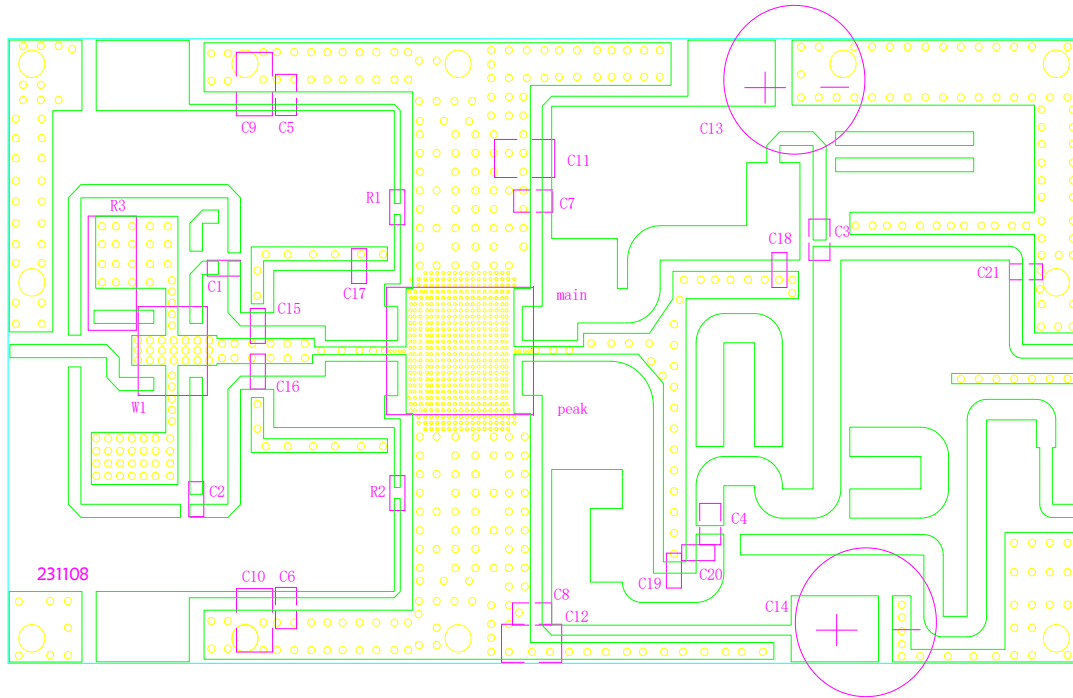


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Designator	Footprint	Comment	Quantity
C1, C2, C19	0603	6.8 pF	3
C3, C4, C5, C6, C7, C8	0603/0805	47 pF	6
C9, C10, C11, C12	1210	10uF/100V	4
C13, C14		220uF/63V	2
C15, C16	0603	8.2 pF	2
C17	0603	2.4 pF	1
C18, C20	0603	3.0 pF	
R1,R2	0603	10Ω	2
R3	2512	51Ω	1
W1		DC07F02 (YANTEL 2dB)	1

TYPICAL CHARACTERISTICS

Figure 5. Power Gain and Drain Efficiency as function of Power Output at Idq=100mA

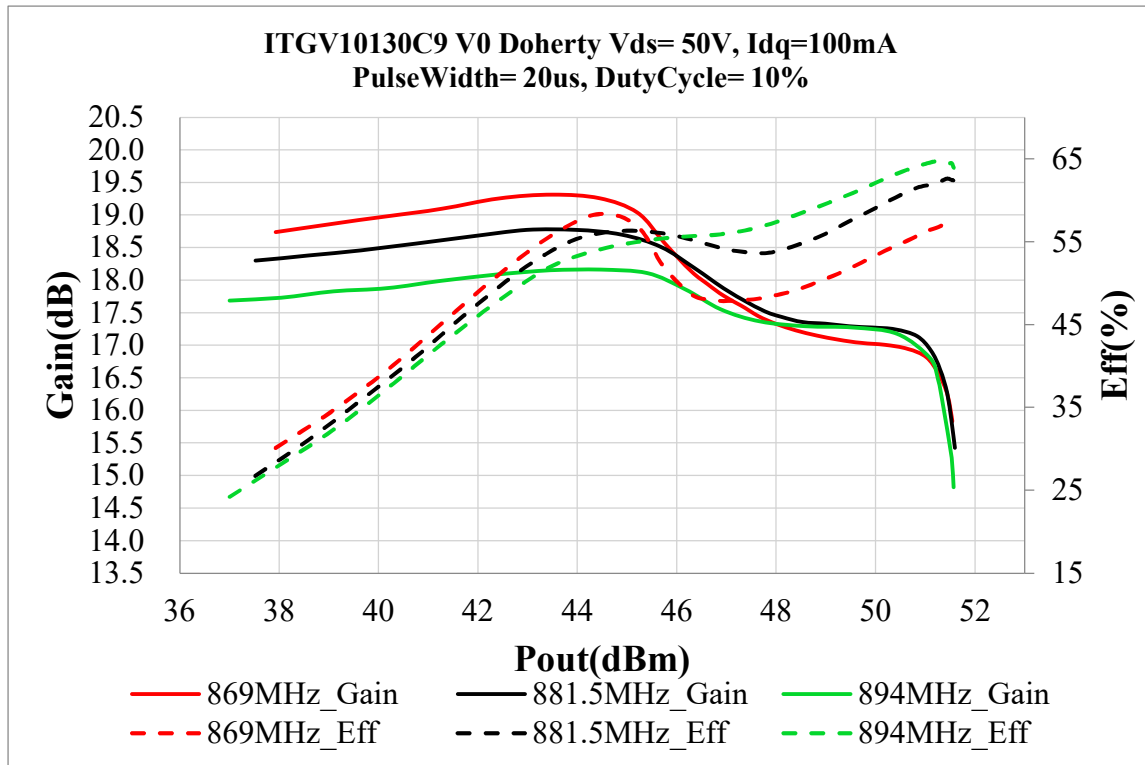
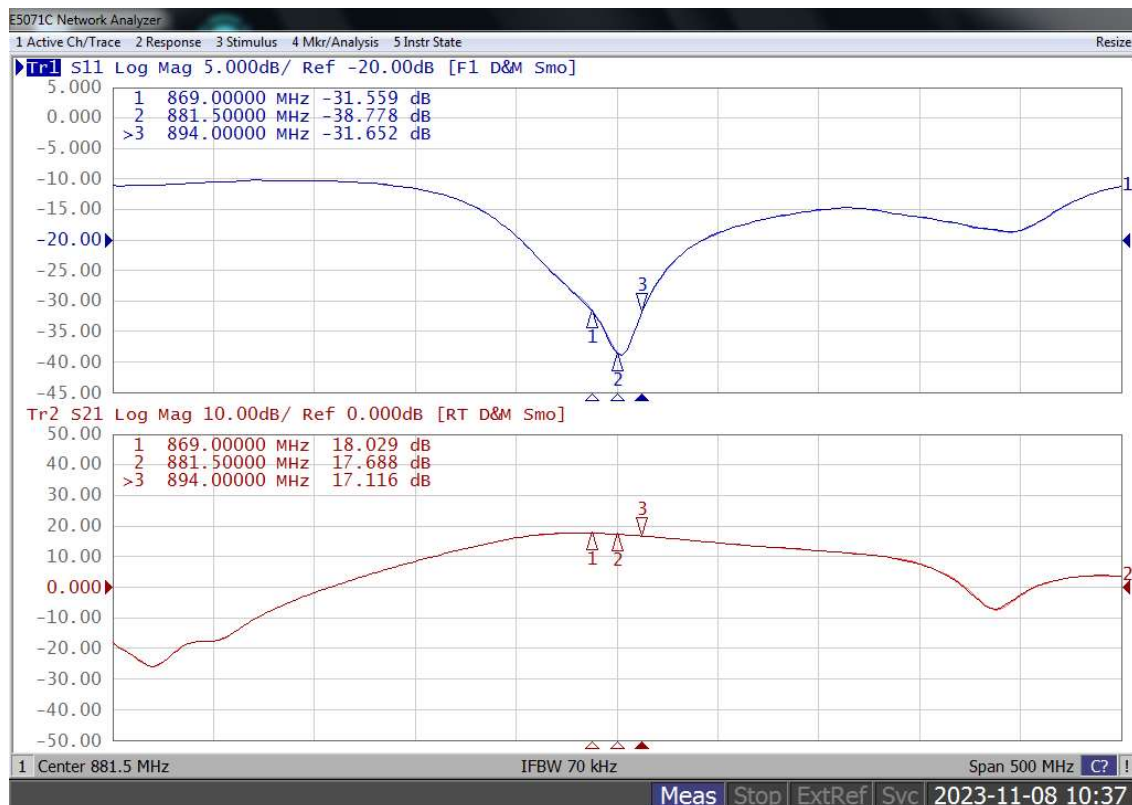
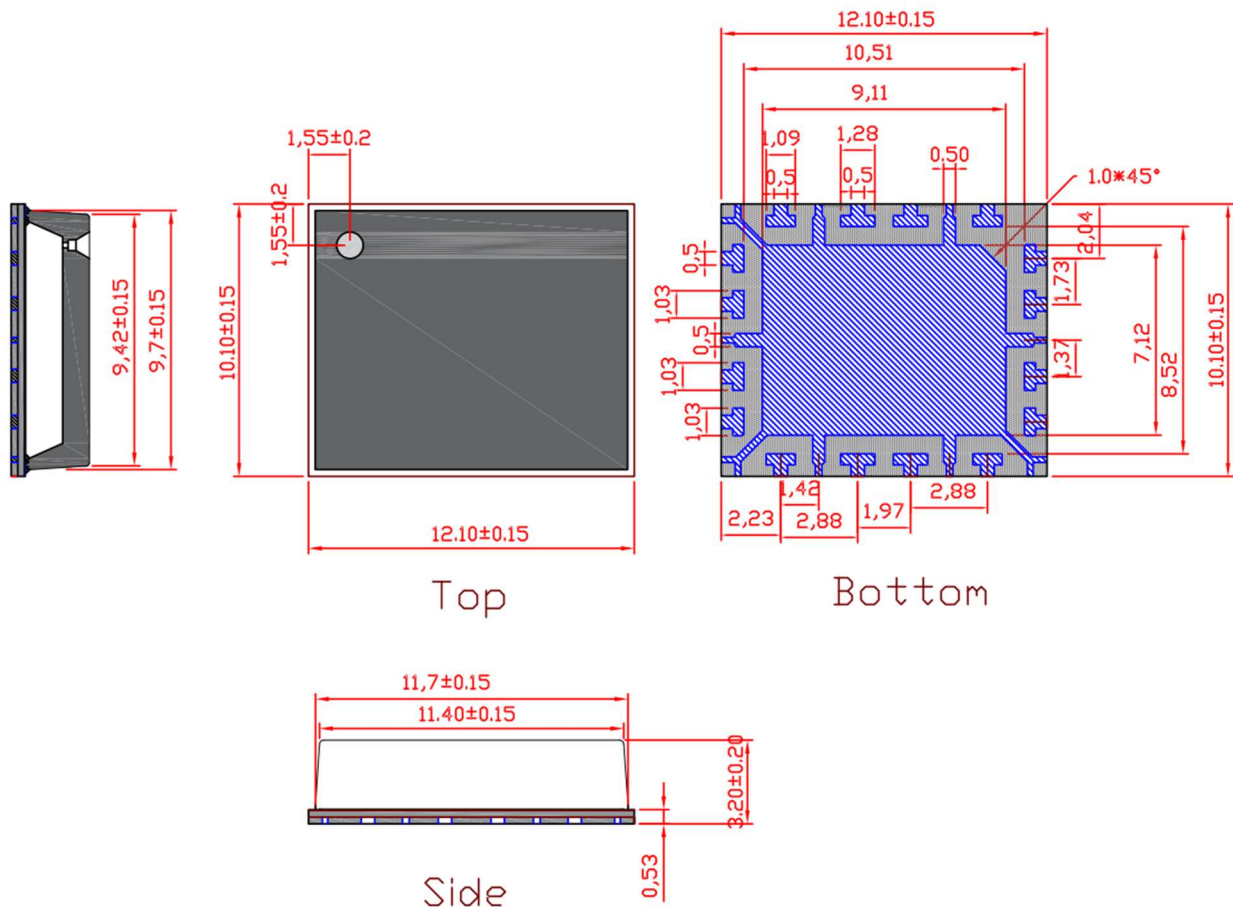


Figure 5. Network analyzer output S11/S21





Package Dimensions (Unit:mm)



Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2023/11/8	Rev 1.0	Preliminary Datasheet
2024/1/4	Rev 1.1	Modify the typo of pin definition on page 2

Application data based on LSM-23-35

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