



Gallium Nitride 50V, 330W, DC-2GHz RF Power Transistor

Description

The SL2033VS is a 330W, **single ended** GaN HEMT, designed for multiple applications with frequencies up to 2GHz. It is optimized thermally to support CW application.

There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.

- VDS=50V Vgs=-3.17V Idq=320mA on wideband application board with device soldered

Signal mode: Pulsed CW, 20us width, 10% duty cycle.

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff (%)	P1dB Gain (dB)	P3dB (dBm)	P3dB (W)	P3dB Eff (%)
750	55.88	387.2	65.8	22.08	57.09	512.0	74.7
800	54.71	296.0	61.7	21.88	56.41	437.1	73.5
850	53.97	249.2	64.3	22.08	55.71	372.3	75.6
900	55.07	321.0	66.7	21.34	56.56	453.4	76.5
950	54.98	314.8	64.1	20.41	56.56	453.3	74.1
1000	55.13	325.6	62.3	20.73	56.72	469.7	72.2

Signal mode: CW, Pin=36dBm

Freq (MHz)	Pout (W)	Power Gain (dB)	Eff (%)
750-1000	>330	>19	>65%



Applications

- L band power amplifier application
- P band power amplifier application

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

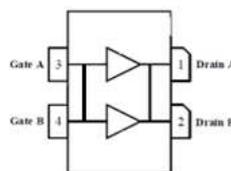
1. Set VGS to the pinch-off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)



***Notice: Both leads at input and output are internally connected, device is only usable as single ended**



Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	32	Vdc
Maximum gate current	I_{gs}	43.2	mA
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_C=85^\circ\text{C}$, at $P_d=150\text{W}$,	$R_{\theta JC}$	0.7	°C /W

Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS}=-8\text{V}$; $I_{DS}=43.2\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS}=10\text{V}$, $I_D=43.2\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS}=50\text{V}$, $I_{DS}=350\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.13		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	50V 2GHz, $P_{out}=330\text{W}$ pulsed CW, All phase, No device damages	VSWR		10:1		

Figure 2: Network analyzer output, S11 and S21

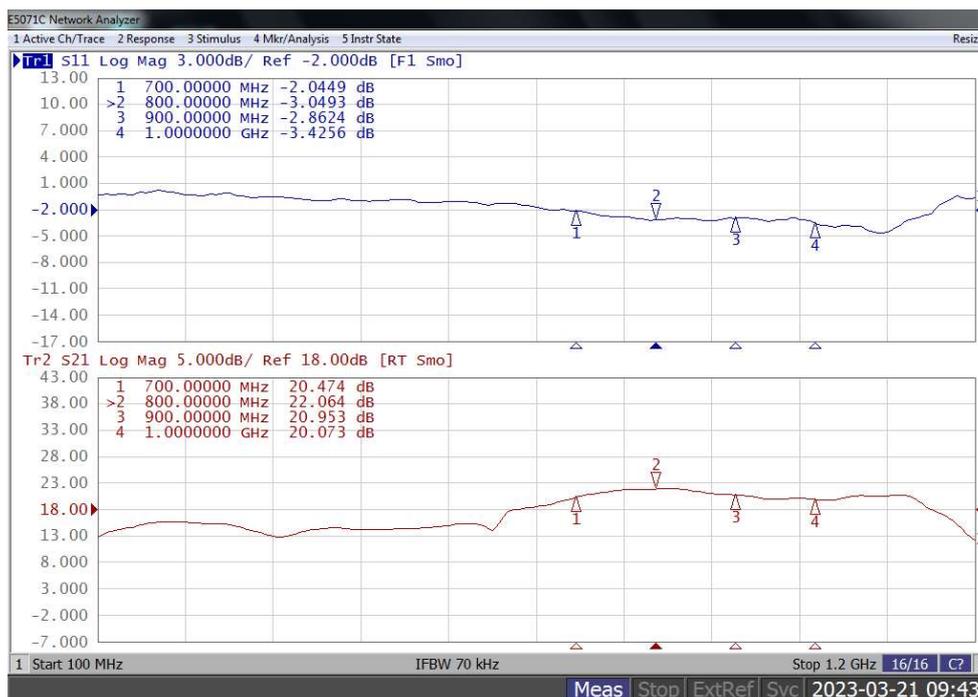


Figure 4: Picture of application board for 0.7-1GHz Class AB

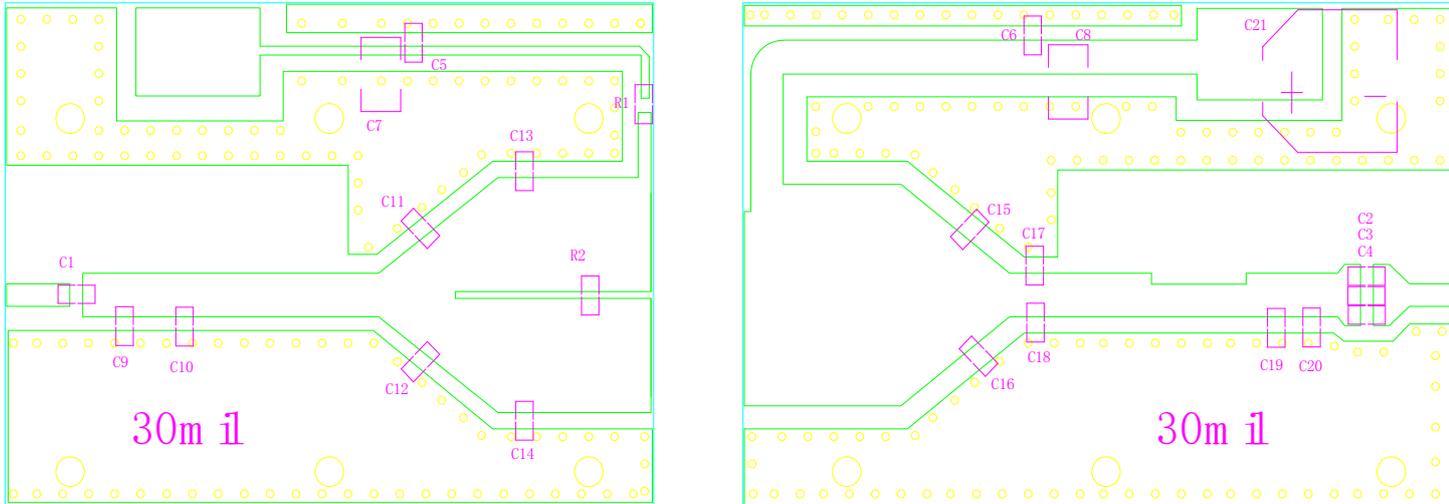


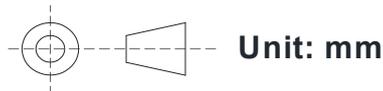
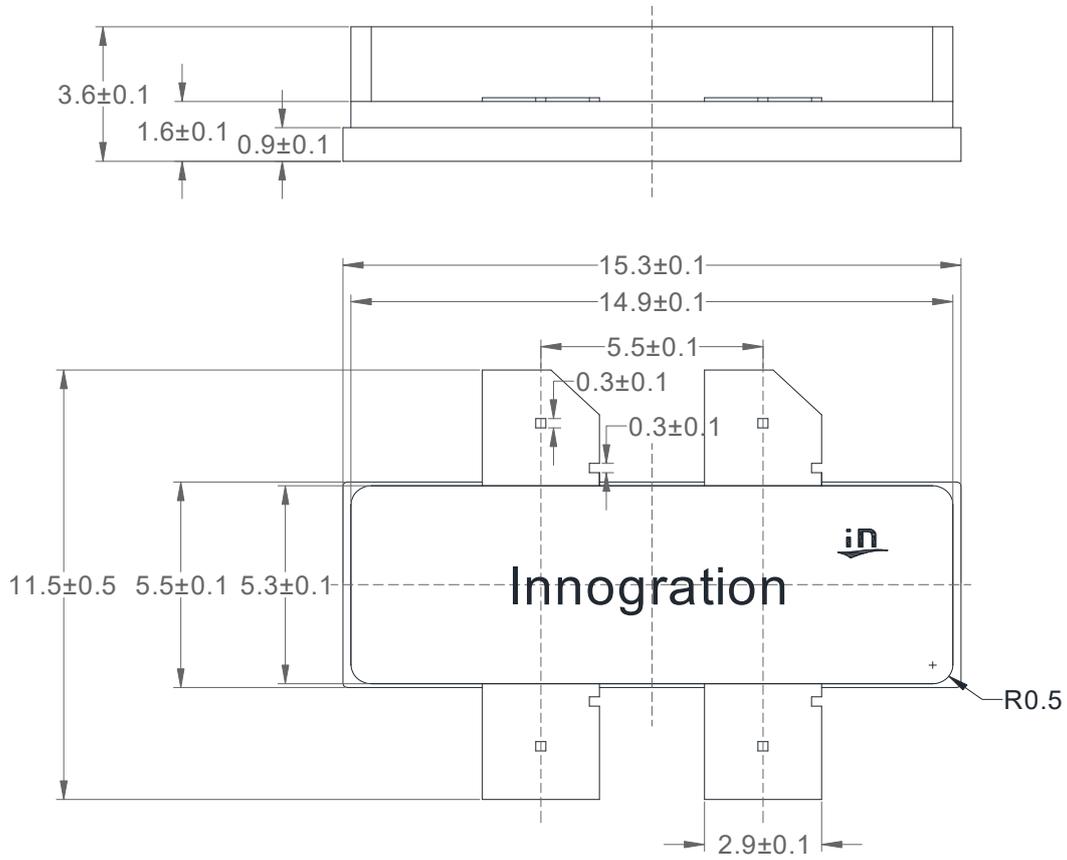
Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 30Mils)

Designator	Footprint	Comment	Quantity
C1	0805	10pF	1
C2, C3, C4	0805	18pF	3
C5, C6	0805	43pF	3
C7, C8	1210	10uF/100V	2
C9, C10, C17, C18, C19	0805	2.4pF	5
C20	0805	1.5pF	1
C21		100uF/63V	1
R1, R2	0603	10R	2

(pF capacitors are ATC 600F series)



Earless Flanged Ceramic Package; 4 leads





Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2022/12/14	V1.0	Production Datasheet Creation
2023/3/21	V1.1	Change PCB layout for more thermally friendly

Application data based on LSM-23-07/12

Notice

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