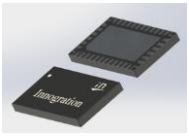
DC-0.5GHz, 25W, 50V LDMOS Fully matched PA Module



Description

The IMGV0005-25 is a 25-watt ,single stage integrated Power Amplifier Module, designed for broad band applications, with frequencies from DC to 0.5GHz. The module is 50 Ω input/output matched and requires minimal external components.

The module implements distributed power amplifier in form of multi chips, housed in cost effective plastic open cavity package, offers a much lower cost than traditional MMIC solutions.

Vds=50V, Idq=150mA, CW **with bias solution 1**

Parameter	13.56MHz	30MHz	100MHz	200MHz	300MHz	400MHz	500MHz	600MHz	Units
Linear Gain	19.9	18.8	18.1	17.9	18.3	18.6	18.4	18.2	dB
Gain@Pin=30dBm	14.8	14.6	14.6	14.5	14.7	14.6	14.5	14.1	dB
Pout@Pin=30dBm	31.3	29.2	29.1	28.5	29.7	28.7	28.0	25.7	W
Eff@Pin=30dBm	75	79	76	67	62	54	50	44	%

Vds=50V, Idq=150mA, CW **with bias solution 2**

Parameter	1MHz	2MHz	3MHz	4MHz	5MHz	6MHz	7MHz	8MHz	9MHz	Units
Linear Gain	17.8	17.8	17.9	17.9	17.9	17.9	17.9	17.9	17.9	dB
Gain@Pin=28dBm	15.0	15.3	15.4	15.6	15.7	15.8	15.8	15.8	15.8	dB
Pout@Pin=28dBm	20.0	21.3	22.1	23.0	23.5	23.8	24.0	24.0	24.1	W
Eff@Pin=28dBm	57	62	65	68	70	71	72	72	72	%

Parameter	10MHz	20MHz	50MHz	100MHz	200MHz	300MHz	400MHz	500MHz	Units
Linear Gain	17.9	18.0	18.5	20.2	18.8	19.5	19.5	19.4	dB
Gain@Pin=28dBm	15.8	15.9	16.1	16.3	16.1	16.3	16.2	16.4	dB
Pout@Pin=28dBm	24.2	24.6	25.9	27.0	25.9	27.0	26.4	24.1	W
Eff@Pin=28dBm	73	74	74	72	65	58	52	45	%

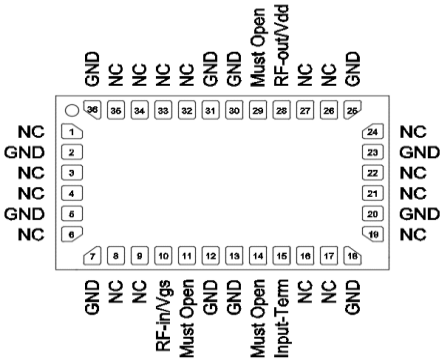
Product Features

- Operating Frequency Range: DC-0.5GHz
- Operating Drain Voltage: +50 V
- 50 Ω Input/Output
- Psat: ≥25W
- Small signal gain:>17dB, Power gain:>14dB
- Minimum efficiency:>50%
- 6x10 mm Surface Mount Package
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC
- Much lower cost than GaN-based ultrawide band PA , due to LDMOS technology used

Applications

- Ultra Broadband Amplifiers
- Driver for ISM, FM
- Test Instrumentation
- EMC Amplifier Drivers
- HF/VHF 2-way Radios

Pin Configuration and Description



Top View

Pin No.	Symbol	Description
28	RFout/Vdd	Transistor 1, Drain Bias & RF Output
10	RFin/Vgs	Transistor 1, RF Input &Gate Bias
15	Input-Term	Transistor 1, Input 50 ohm term
Others	NC	No connection
11, 14, 29	Must Open	Keep the pin open, no GND
2,5,7,12,13,16,20,23,25, 30, 31,36 Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+50	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 25°C, DC test	RθJC	1.7	°C/W

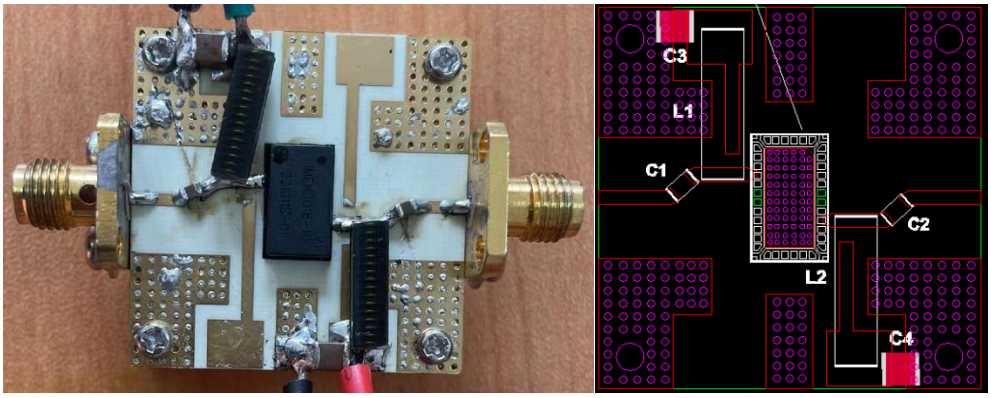
Table 3. Electrical Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range	Pin=30dBm	1		500	MHz
Power Gain @ Psat	Pin=30dBm	14			dB
P_{SAT}	Pin=30dBm	44			dBm
Drain Efficiency @ P_{SAT}	Pin=30dBm	50			%
Unless otherwise noted: TA = 25°C, V_{DD} =50 V, Pulse Width=100 us, Duty cycle=10%					

Load Mismatch of per Section (On Test Fixture, 50 ohm system): V_{DD} =50 V, I_{DQ} =150 mA, f = 0.5GHz

VSWR 10:1 at Psat pulse CW Output Power	No Device Degradation

Reference Circuit of Test Fixture Assembly Diagram with bias solution 1



		Part NO.	Vendor
C3,C4	10uF 100V Chip Capacitor	C5750X7S2A106M230KB	TDK
C1,C2	50V 1uF Chip Capacitor	GRM21BR71H105KA12L	muRata
L1,L2	1.3uH 4.2A Inductor	4310LC-132KEC	Coilcraft
PCB	RO4350B,20mil,er=3.48		

TYPICAL CHARACTERISTICS

Figure 1. Network analyzer output S11/S21 (Pin=0dBm)

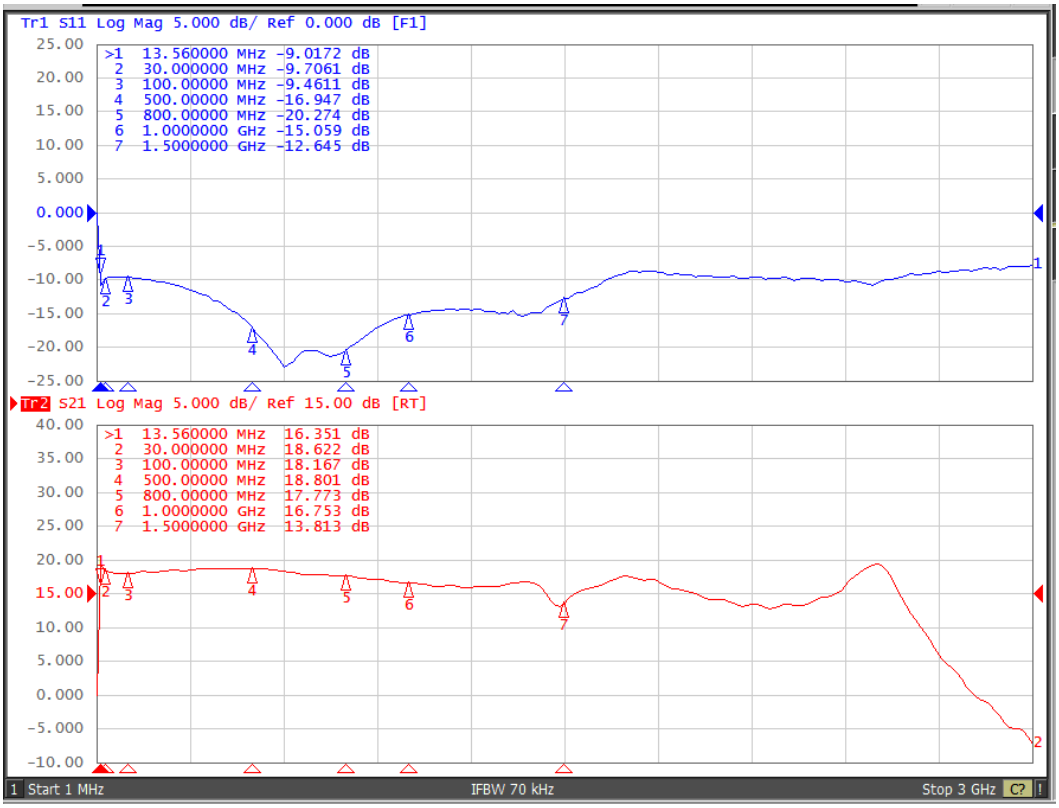
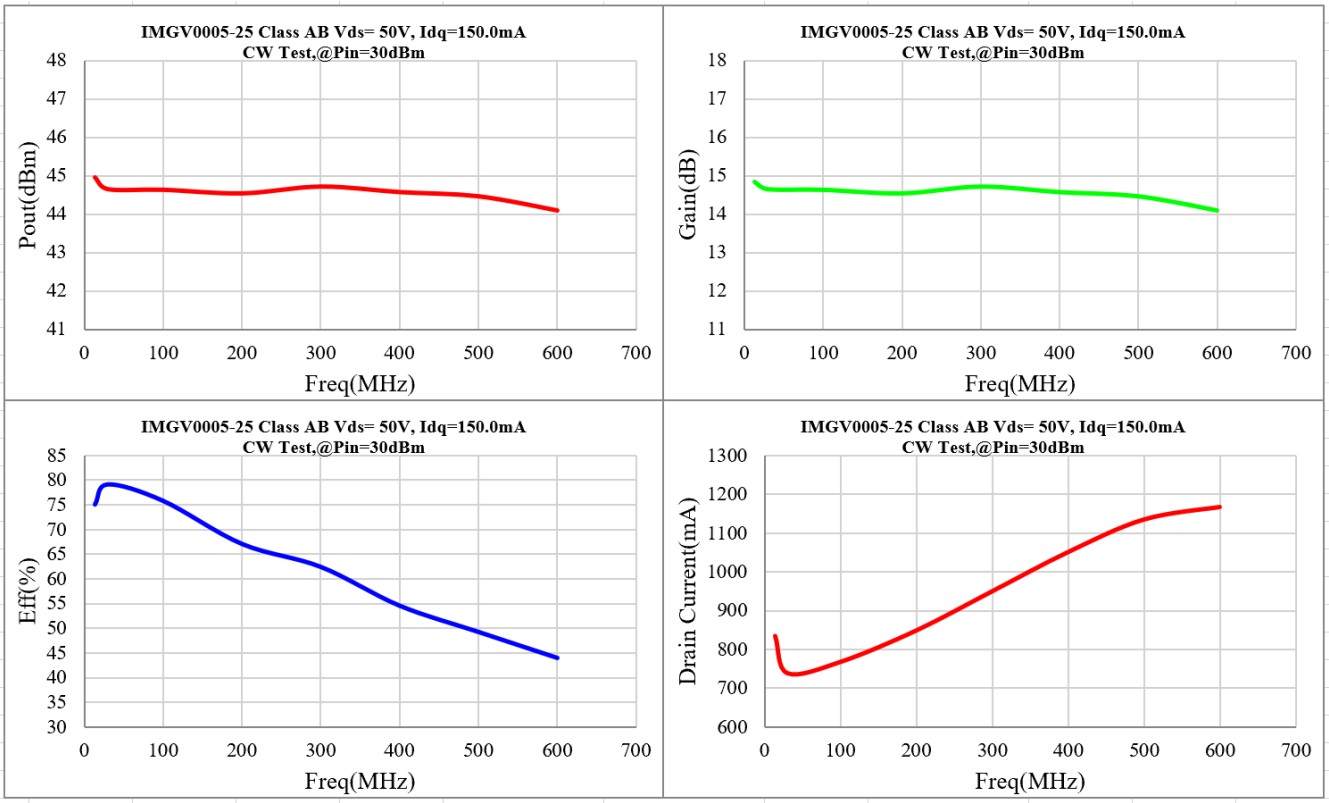
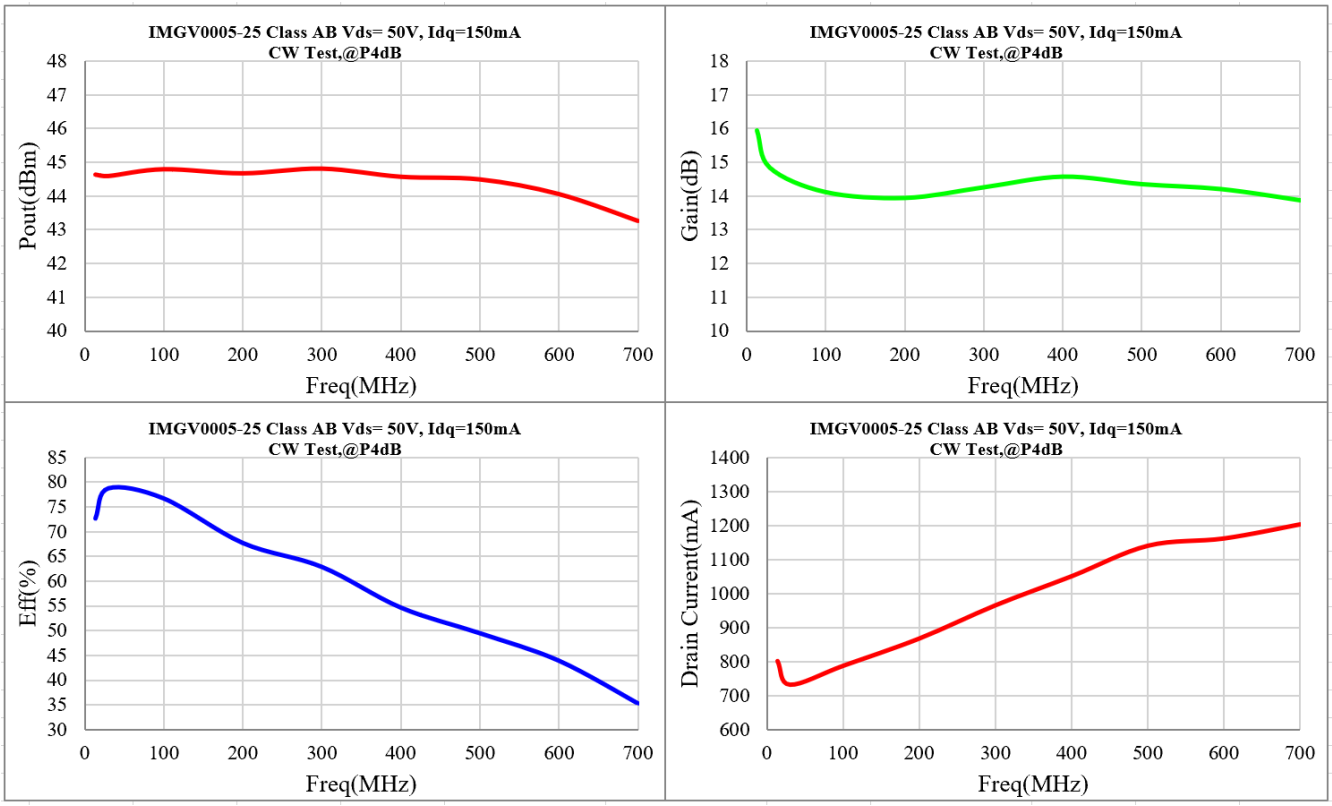


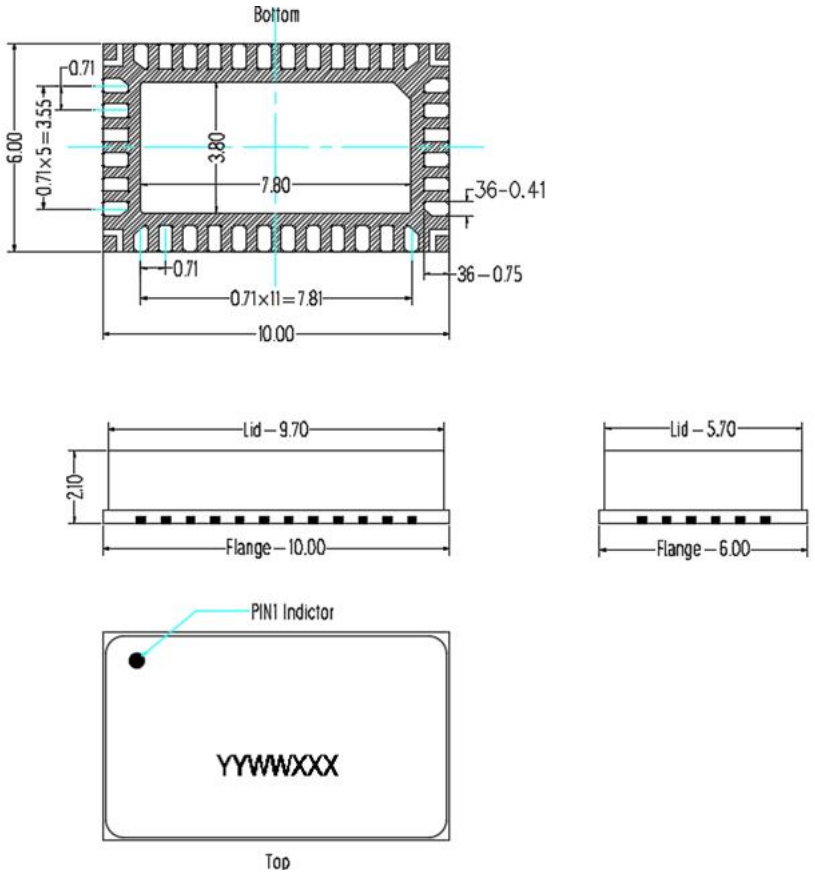
Figure. Power Gain and, efficiency and Pout @Pin=30dBm ,and P4dB vs. Frequency





Package Dimensions

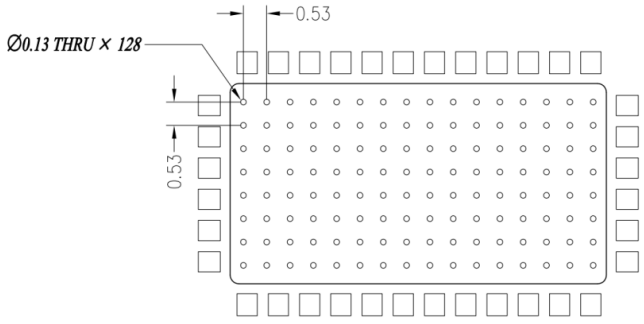
10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.2mm.

Mounting Footprint Pattern



Notes:

1. All dimensions are in mm;
2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. ALL vias are PTH to ground.

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2023/3/29	Rev 1.0	Production Datasheet
2025/5/27	Rev 1.1	Add application info of bias solution 2 ,down to 1MHz as start

Application data based on ZHH-23-06/25-10

Disclaimers

Specifications are subject to change without notice. Innogration believes the information contained within this data sheet to be accurate and reliable. However, no responsibility is assumed by Innogration for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Innogration . Innogration makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose.“Typical” parameters are the average values expected by Innogration in large quantities and are provided for information purposes only. These values can and do vary in different applications and actual performance can vary over time. All operating parameters should be validated by customer’s technical experts for each application. Innogration products are not designed, intended or authorized for use as components in applications intended for surgical implant into the body or to support or sustain life, in applications in which the failure of the Innogration product could result in personal injury or death or in applications for planning, construction, maintenance or direct operation of a nuclear facility. For any concerns or questions related to terms or conditions, pls check with Innogration and authorized distributors