

# ITEV05500B4 LDMOS TRANSISTOR

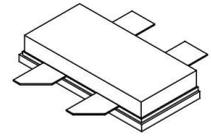
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Product Datasheet V1.0

## 500W,433MHz, 50V High Power RF LDMOS FETs

### Description

The ITEV05500B4 is a 500-watt capable, high performance, matched LDMOS FET, designed for 433MHz RF Energy and ISM application. It can be used for both CW and pulse application.

**ITEV05500B4**



- Typical Performance (On Innogration 433MHz fixture with device soldered):

V<sub>DS</sub>= 50V, I<sub>DQ</sub>=50mA(V<sub>GS</sub>=3.1V), CW

Freq (MHz)	Power Gain(dB)	Pout (dBm)	Pout (W)	Eff (%)
433	21	57.2	520	74.3

### Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- On chip RC network enable high stability and ruggedness
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	V <sub>DSS</sub>	115	Vdc
Gate--Source Voltage	V <sub>GS</sub>	-7 to +10	Vdc
Operating Voltage	V <sub>DD</sub>	+52	Vdc
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Case Operating Temperature	T <sub>c</sub>	+150	°C
Operating Junction Temperature	T <sub>j</sub>	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 80°C, 500W CW, 50 Vdc, I <sub>DQ</sub> = 100 mA	R <sub>θJC</sub>	0.25	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

**Table 4. Electrical Characteristics** (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### DC Characteristics (Per Side)

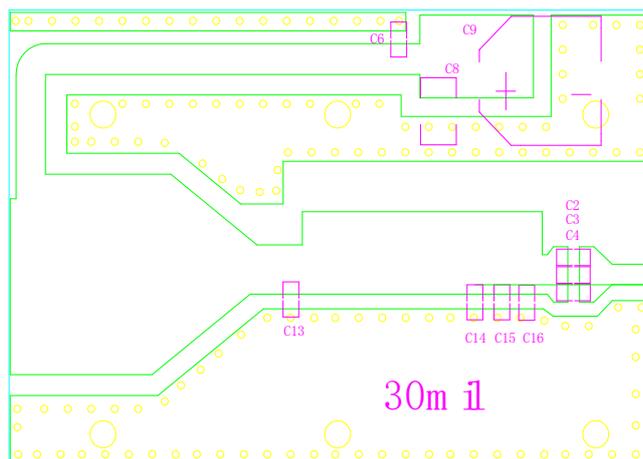
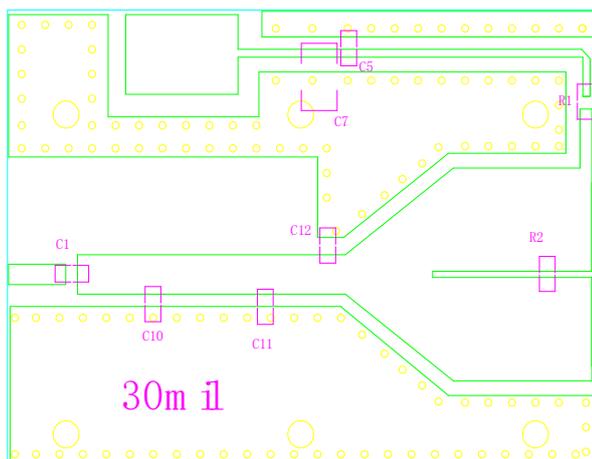
Drain-Source Voltage V <sub>GS</sub> =0, I <sub>DS</sub> =18.0mA	V <sub>(BR)DSS</sub>		115		V
Zero Gate Voltage Drain Leakage Current (V <sub>DS</sub> = 50V, V <sub>GS</sub> = 0 V)	I <sub>DSS</sub>			1	μA
Gate—Source Leakage Current	I <sub>GSS</sub>			1	μA

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( $V_{GS} = 10\text{ V}$ , $V_{DS} = 0\text{ V}$ )				
Gate Threshold Voltage ( $V_{DS} = 50\text{ V}$ , $I_D = 600\ \mu\text{A}$ )	$V_{GS(th)}$		2.6	V
Gate Quiescent Voltage ( $V_{DD} = 50\text{ V}$ , $I_D = 100\text{ mA}$ , Measured in Functional Test)	$V_{GS(Q)}$		32	V

## Reference Circuit of Test Fixture (433MHz)



Designator	Footprint	Comment	Quantity
C1	0805	8.2pF	1
C2, C3, C4(*)	0805	100pF	3
C5	0805	100pF	1
C6	1210	100pF	1
C7, C8	1210	10uF/100V	2
C9		100uF/63V	1
C10, C11	0805	15pF	2
C12, C13, C15, C16	0805	10pF	4
C14	0805	6.8pF	1
R1, R2	0603	10R	2

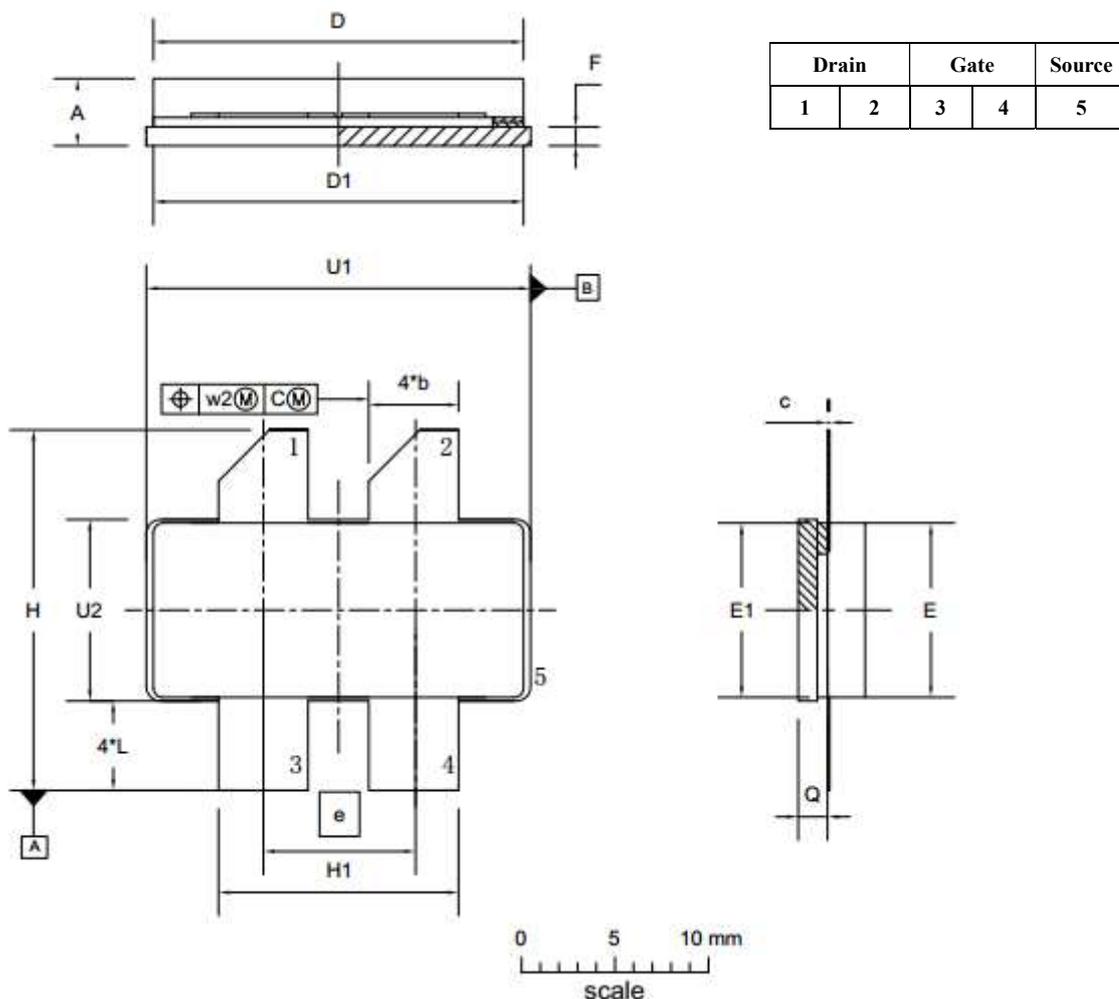
(\* or 2X 1210-100pF)

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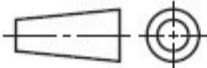
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## Package Outline

Earless Flanged Ceramic Package; 4 leads



UNIT	A	b	c	D	D <sub>1</sub>	e	E	E <sub>1</sub>	F	H	H <sub>1</sub>	L	Q	U <sub>1</sub>	U <sub>2</sub>	W <sub>1</sub>	W <sub>2</sub>
mm	4.72	4.67	0.15	20.02	19.96	7.90	9.50	9.53	1.14	19.94	12.98	5.33	1.70	20.70	9.91	0.25	0.51
	3.43	4.93	0.08	19.61	19.66		9.30	9.25	0.89	18.92	12.73	4.32	1.45	20.45	9.65		
inches	0.186	0.194	0.006	0.788	0.786	0.311	0.374	0.375	0.045	0.785	0.511	0.210	0.067	0.815	0.390	0.01	0.02
	0.135	0.184	0.003	0.772	0.774		0.366	0.364	0.035	0.745	0.501	0.170	0.057	0.805	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013

## Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/4/11	Rev 1.0	Preliminary Datasheet

Application data based on LSM-23-15

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