

MC2515S LDMOS TRANSISTOR

Document Number: MC2515S
Product Datasheet V1.1

150W, S band High Power RF LDMOS FETs

Description

The MC2515S is a 150watt, internally matched, single ended LDMOS FETs, designed for S band commercial application within 2100-2500MHz. It can be used in Class AB/B and Class C for any pulse signal or CW signal

• Typical Performance (On Innogration fixture with device soldered):

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MC2515S VDS=28V Idq=100mA Vgs=2.43V CW						
F(MHz)	Pin (dBm)	Psat (dBm)	Psat (W)	I(A)	Gain (dB)	Eff(%)
2100	43	53.11	205	15.90	10.1	46.0
2150	42	53.45	221	17.00	11.5	46.5
2200	41	53.53	226	16.10	12.5	50.1
2250	41.5	53.50	224	15.80	12.0	50.7
2300	40.35	53.42	220	15.10	13.1	52.0
2350	42.2	53.52	225	14.80	11.3	54.3
2400	41.3	52.80	191	13.80	11.5	49.3
2450	42.1	52.82	191	13.96	10.7	49.0
2500	42.5	52.60	182	13.50	10.1	48.1

When used at 32V, it can deliver 200W power across the full band

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- S band pulse CW amplifier
- ISM applications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C=85^{\circ}\text{C}$, $T_J=200^{\circ}\text{C}$, DC test	$R_{\theta JC}$	0.2	°C/W

Table 3. ESD Protection Characteristics

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Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Zero Gate Voltage Drain Leakage Current (V _{DS} = 65V, V _{GS} = 0 V)	I _{loss}			100	μA
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 V, V _{GS} = 0 V)	I _{loss}			1	μA
Gate--Source Leakage Current (V _{GS} = 10 V, V _{DS} = 0 V)	I _{gss}			1	μA
Gate Threshold Voltage (V _{DS} = 28V, I _D = 450 μA)	V _{GS(th)}		1.9		V
Gate Quiescent Voltage (V _{DD} = 28 V, I _D = 100 mA, Measured in Functional Test)	V _{GS(q)}		2.4		V

Figure 1. Test Circuit Component Layout

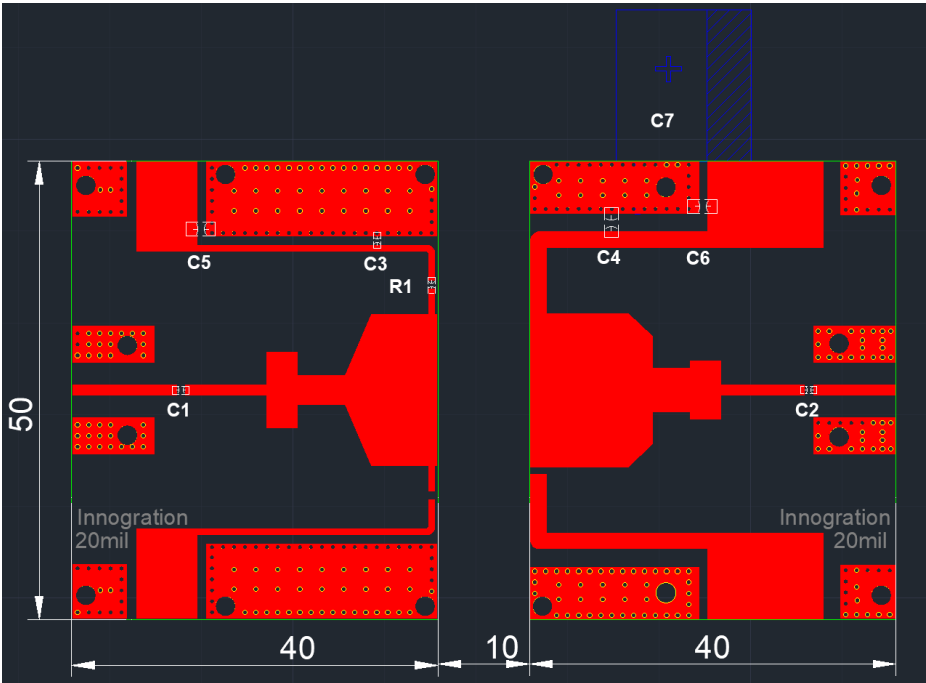


Table 4. Test Circuit Component Designations and Values

Part	description	Model
R1	7.50Ω	Chip Resistor
C1 ,C3	15PF 600F	
C2	22PF ATC 800R	

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C4	12PF MQ10111	
C7	470UF/63V	
C5,C6	10uF 1210	
PCB	20mil Rogers4350B	

Package Outline

Flangeless ceramic package;

INP-688-2-EL (C2)

Technical drawing of the INP-688-2-EL (C2) package showing top, side, and bottom views with dimensions.

Top View Dimensions:

- Top edge: 0.5000
- Right edge: 1.5200
- Bottom edge: $15.840 \pm .127$ [$0.624 \pm .005$]
- Left edge: $9.780 \pm .127$ [$0.385 \pm .005$]
- Top-left corner: $(45^\circ \times 2.72$ [$.107$])
- Top-right corner: 0.5000
- Bottom-right corner: $4XR.88$ [$R0.035$]
- Bottom-right corner: $4XR.63$ [$R0.025$]

Side View Dimensions:

- Top edge: $9.400 \pm .127$ [$0.370 \pm .005$]
- Right edge: $19.430 \pm .127$ [$0.766 \pm .005$]
- Bottom edge: $1.570 \pm .127$ [$0.062 \pm .005$]

Bottom View Dimensions:

- Top edge: $22.350 \pm .127$ [$0.881 \pm .005$]
- Right edge: $3.670 \pm .3$ [$0.145 \pm .0118$]
- Bottom edge: $23.120 \pm .127$ [$0.911 \pm .005$]

Material specification: $[0.0381 \pm .0015] \text{--} A$

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/5/10	Rev 1.0	Product Datasheet Creation

Application data based on SXY-23-19

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