

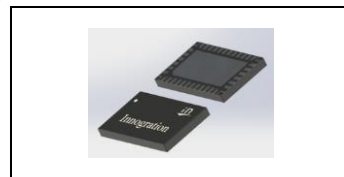


## 0.1-6.0GHz, 2 stages, 8W, 28V GaN Fully matched PA Module

### Description

The G2MAH0160-8 is a 10-watt ,2 stage integrated Power Amplifier Module, designed for broad band applications, with frequencies from 100MHz to 6.0GHz. The module is 50  $\Omega$  input/output matched and requires minimal external components.

The module implements distributed power amplifier in form of multi chips, housed in cost effective plastic open cavity package, offers a much lower cost than traditional MMIC solutions.



- $V_{ds}=28V$ ,  $I_{dq1}=10\text{ mA}$ ,  $I_{dq2}=40\text{ mA CW}$

| Parameter      | 0.1GHz | 1.0GHz | 2.0GHz | 3.0GHz | 4.0GHz | 5.0GHz | 6.0GHz | 6.2GHz | Units |
|----------------|--------|--------|--------|--------|--------|--------|--------|--------|-------|
| Linear Gain    | 24.9   | 22.1   | 22.1   | 20.5   | 19.9   | 21.0   | 21.6   | 21.9   | dB    |
| Gain@Pin=22dBm | 20.3   | 19.7   | 19.9   | 19.0   | 18.5   | 18.0   | 17.9   | 16.7   | dB    |
| Pout@Pin=22dBm | 16.8   | 14.8   | 15.6   | 12.5   | 11.3   | 10.0   | 9.7    | 7.4    | W     |
| PAE@Pin=22dBm  | 59     | 47     | 48     | 35     | 33     | 30     | 38     | 36     | %     |

$V_{ds}=32V$ ,  $I_{dq1}=10\text{ mA}$ ,  $I_{dq2}=40\text{ mA CW}$

| Parameter      | 0.1GHz | 1.0GHz | 2.0GHz | 3.0GHz | 4.0GHz | 5.0GHz | 6.0GHz | 6.2GHz | Units |
|----------------|--------|--------|--------|--------|--------|--------|--------|--------|-------|
| Linear Gain    | 25.3   | 22.6   | 22.6   | 20.7   | 20.2   | 21.4   | 21.9   | 22.5   | dB    |
| Gain@Pin=22dBm | 21.1   | 20.3   | 20.7   | 19.2   | 19.0   | 18.3   | 18.8   | 17.8   | dB    |
| Pout@Pin=22dBm | 20.4   | 17.2   | 18.6   | 13.1   | 12.5   | 10.7   | 12.0   | 9.5    | W     |
| Eff@Pin=22dBm  | 59     | 46     | 44     | 32     | 31.5   | 26     | 37     | 37     | %     |

### Product Features

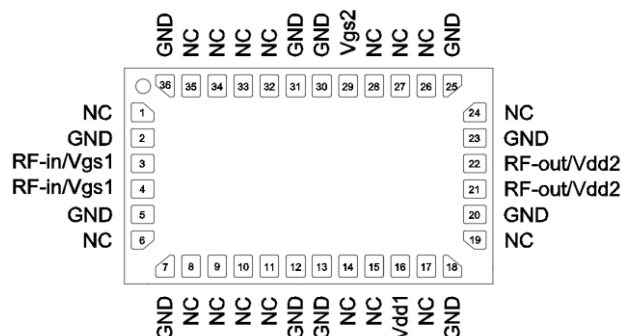
- Operating Frequency Range: 0.1-6.0GHz
- Operating Drain Voltage: +28 V (Up to 32V)
- 50  $\Omega$  Input/Output
- $P_{sat}$ :  $\geq 39\text{dBm}$  @28V,  $\geq 40\text{dBm}$  @32V
- Small signal gain:>19dB, Power gain:>17dB @Pin=22dBm
- Minimum efficiency:>25%
- 6x10 mm Surface Mount Package
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

### Applications

- Ultra Broadband Amplifiers
- Fiber Drivers
- Test Instrumentation
- EMC Amplifier Drivers
- 2-way Radios



## Pin Configuration and Description



| Pin No.                                          | Symbol     | Description                                                                                                                                                                                                |
|--------------------------------------------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 21,22                                            | RFout/Vdd2 | Transistor 1, Drain Bias2 & RF Output                                                                                                                                                                      |
| 3,4                                              | RFin/Vgs1  | Transistor 1, Gate Bias1 & RF Input                                                                                                                                                                        |
| 29                                               | Vgs2       | Transistor 1, Gate Bias2                                                                                                                                                                                   |
| 16                                               | Vdd1       | Transistor 1, Drain Bias1                                                                                                                                                                                  |
| Others                                           | NC         | No connection                                                                                                                                                                                              |
| 2,5,7,12, 13,18,20,23,25, 30, 31,36 Package Base | GND        | DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage. |

Table 1. Maximum Ratings

| Rating                         | Symbol    | Value       | Unit |
|--------------------------------|-----------|-------------|------|
| Drain--Source Voltage          | $V_{DS}$  | 150         | Vdc  |
| Gate--Source Voltage           | $V_{GS}$  | -10 to +2   | Vdc  |
| Operating Voltage              | $V_{DD}$  | +36         | Vdc  |
| Input CW Power                 | RFin      | 25          | dBm  |
| Storage Temperature Range      | $T_{stg}$ | -65 to +150 | °C   |
| Case Operating Temperature     | $T_c$     | +150        | °C   |
| Operating Junction Temperature | $T_j$     | +225        | °C   |

Table 2. Thermal Characteristics

| Characteristic                                                                  | Symbol          | Value | Unit |
|---------------------------------------------------------------------------------|-----------------|-------|------|
| Thermal Resistance, Junction to Case, FEA<br>$T_c = 25^\circ\text{C}$ , DC test | $R_{\theta JC}$ | 4.9   | °C/W |

Table 3. Electrical Characteristics

| Parameter                    | Condition | Min | Typ | Max  | Unit |
|------------------------------|-----------|-----|-----|------|------|
| Frequency Range              |           | 100 |     | 6000 | MHz  |
| Power Gain                   |           | 17  |     |      | dB   |
| $P_{OUT}$                    | Pin=22dBm | 39  | 40  |      | dBm  |
| Drain Efficiency @ $P_{SAT}$ |           | 25  |     |      | %    |

Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 28\text{ V}$ , Pulse Width=100 us, Duty cycle=10%

Load Mismatch of per Section (On Test Fixture, 50 ohm system):  $V_{DD} = 28\text{ V}$ ,  $I_{DQ1+2} = 10+40\text{ mA}$ ,  $f = 3.5\text{ GHz}$

|                                               |                       |
|-----------------------------------------------|-----------------------|
| VSWR 10:1 at pulse CW Output Power @Pin=22dBm | No Device Degradation |
|-----------------------------------------------|-----------------------|

## Reference Circuit of Test Fixture Assembly Diagram

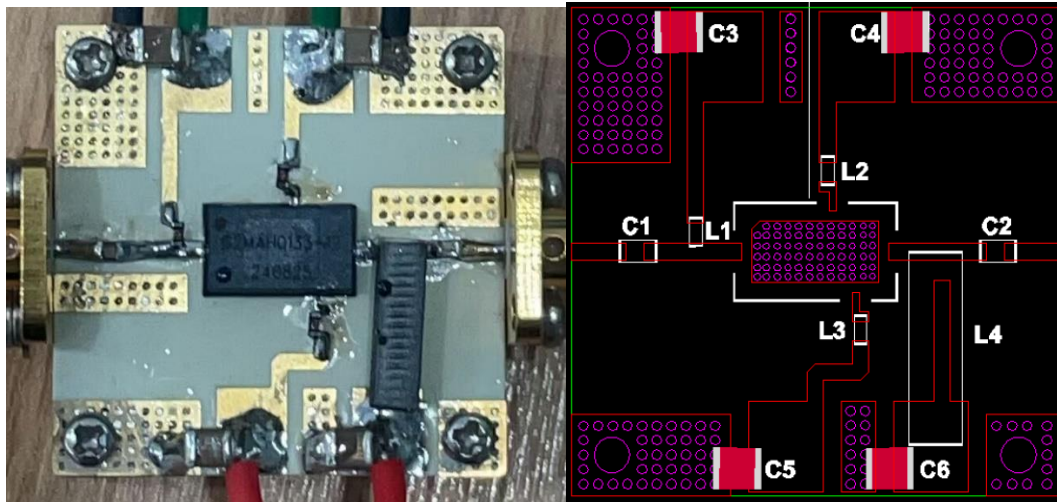


Figure 1. Test Circuit Component Layout

|             |                          | Part NO.            | Vendor    |
|-------------|--------------------------|---------------------|-----------|
| C1, C2      | 50V 1uF Chip Capacitor   | GRM21BR71H105KA12L  | muRata    |
| C3,C4,C5,C6 | 10uF 100V Chip Capacitor | C5750X7S2A106M230KB | TDK       |
| L1, L2,L3   | 100 nH Capacitor(0603)   | LQW18CNR10K00D      | muRata    |
| L4          | 1.3uH 4.2A Inductor      | 4310LC-132KEC       | Coilcraft |
| PCB         | RO4350B,20mil,er=3.48    |                     |           |

## TYPICAL CHARACTERISTICS

Figure 2. Network analyzer output S11/S21 (VDS= 28V, IDQ1=10 mA IDQ1=40 mA, Pin=0dBm)

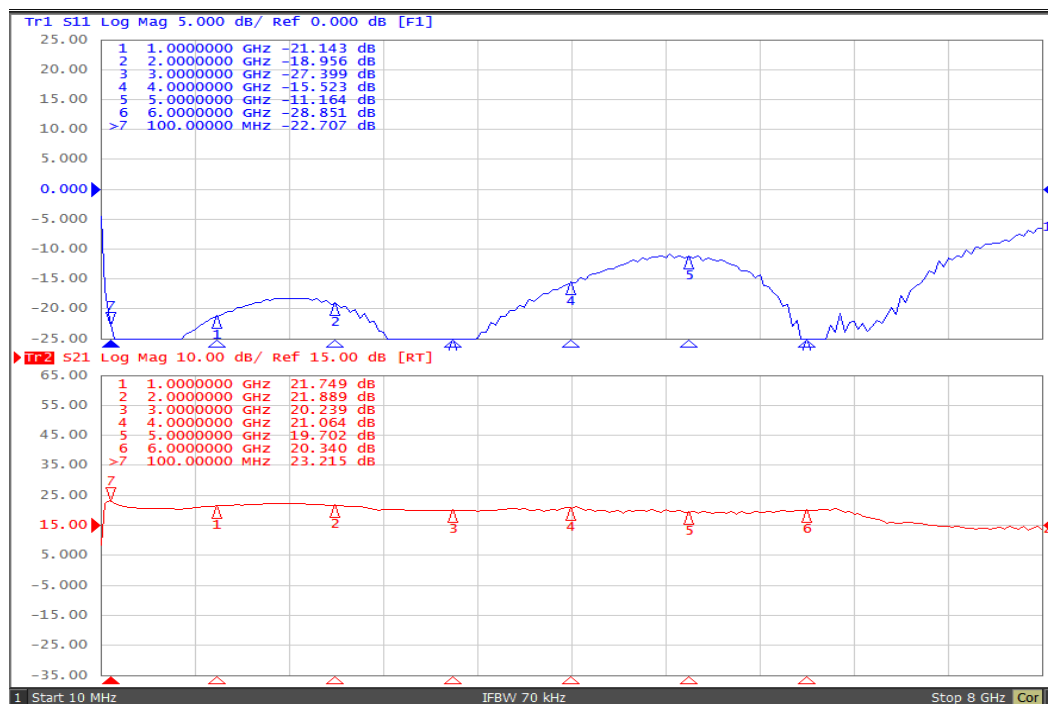


Figure 3. Power Gain and, efficiency and Pout @Pin=22dBm, P4dB vs. Frequency

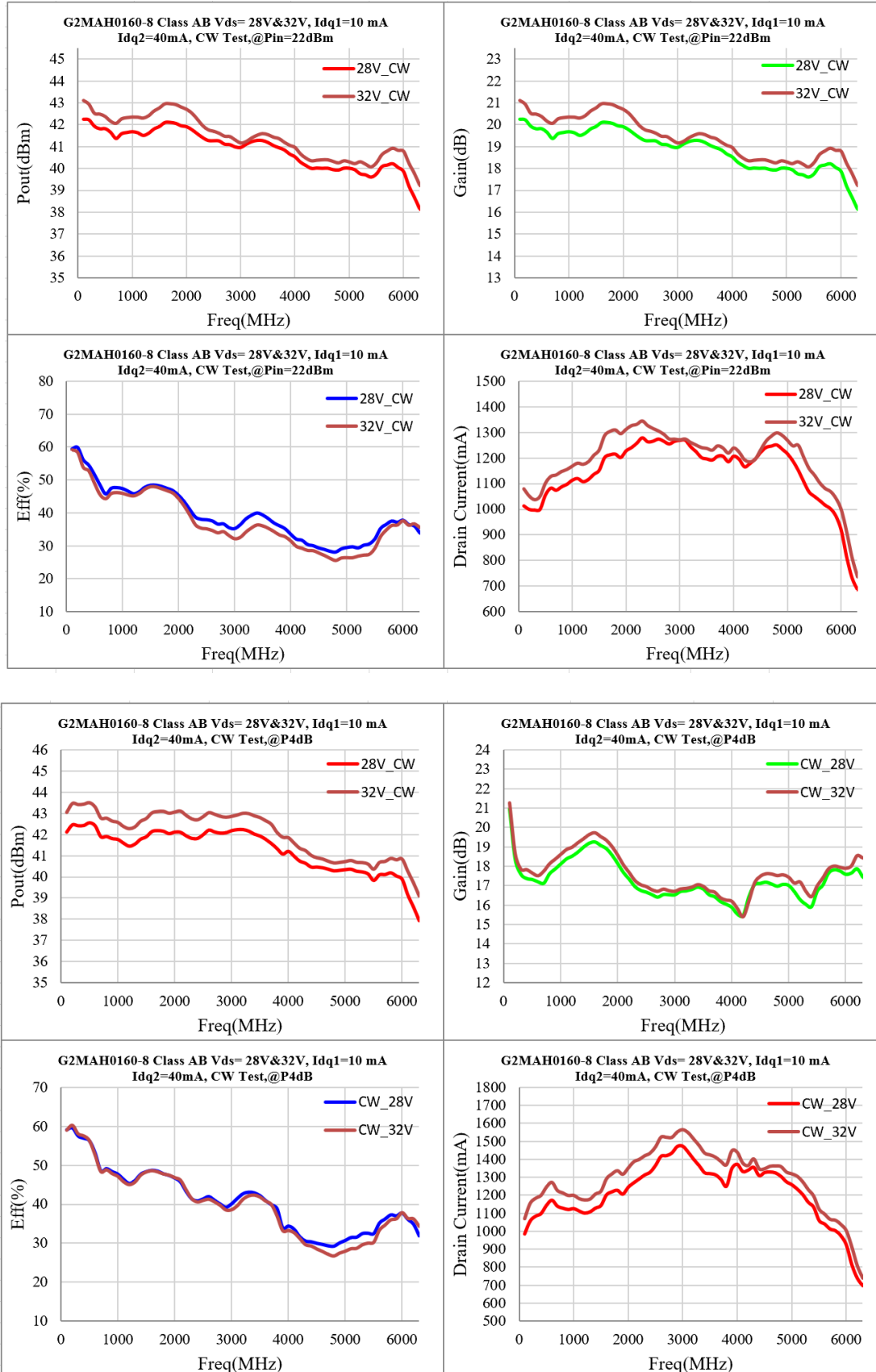
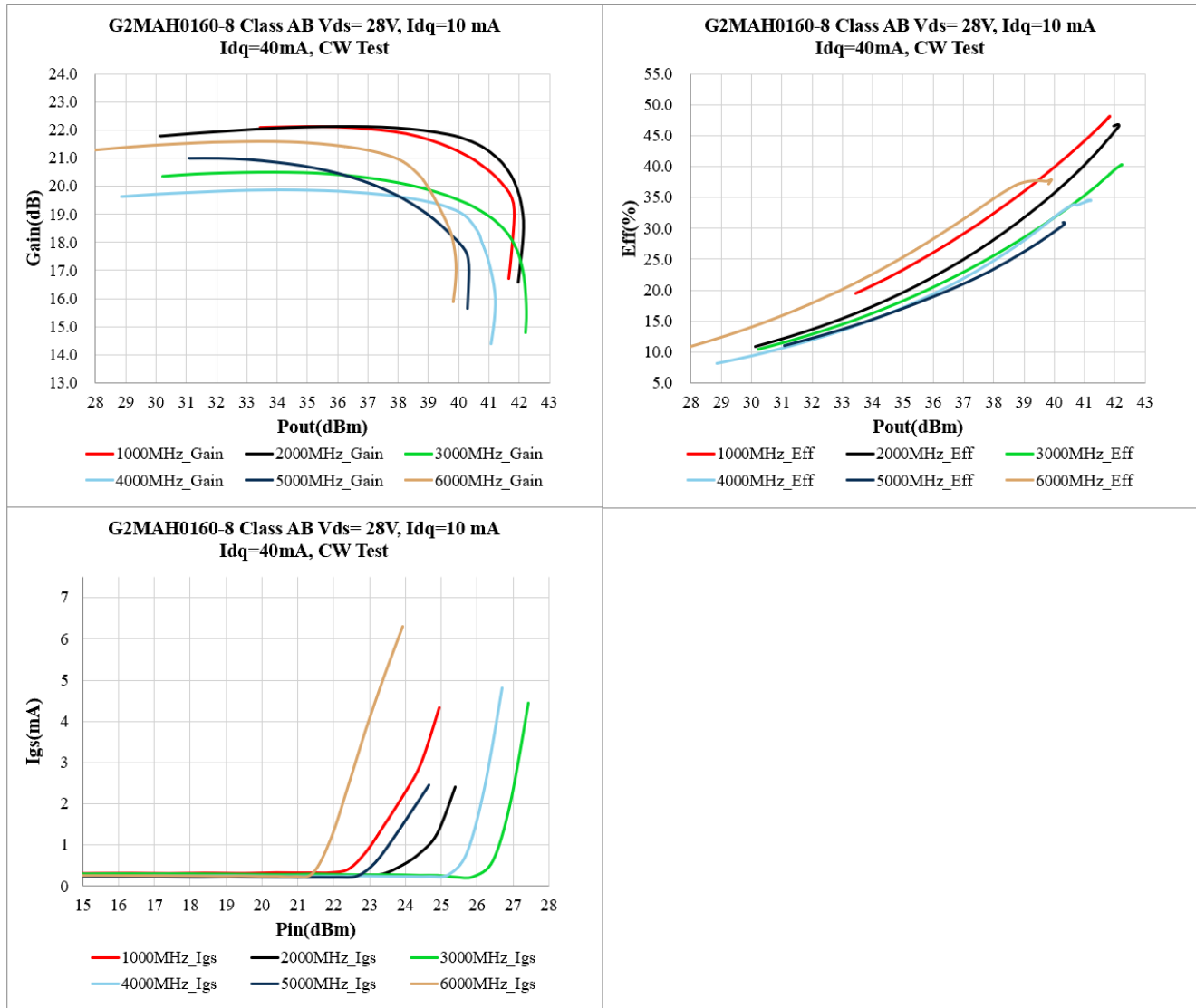
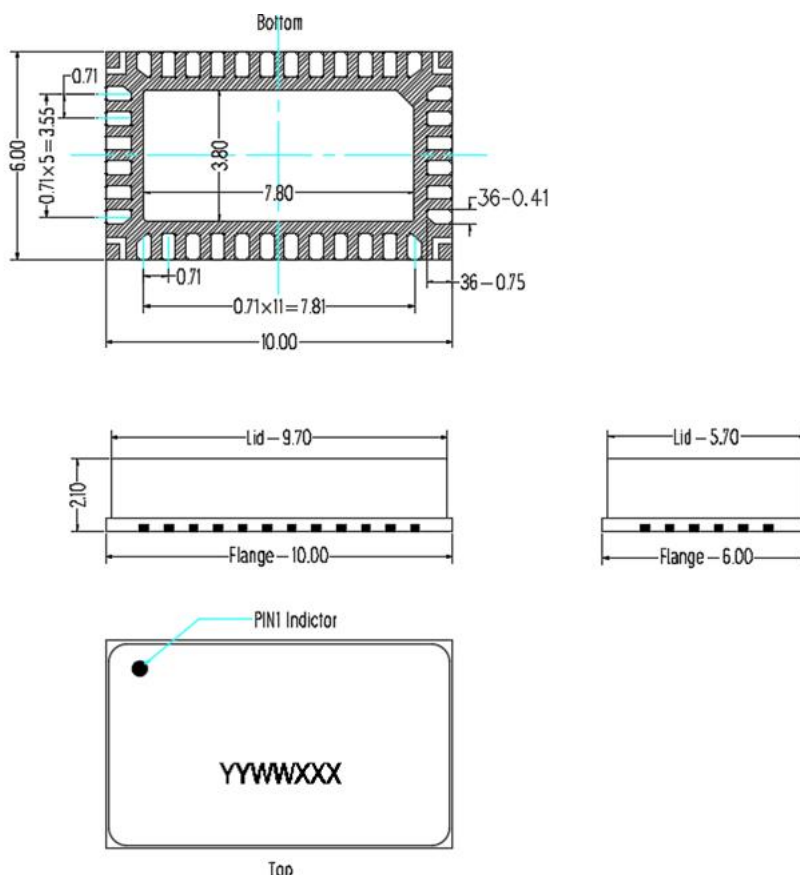


Figure 4. AM/AM Plot



## Package Dimensions

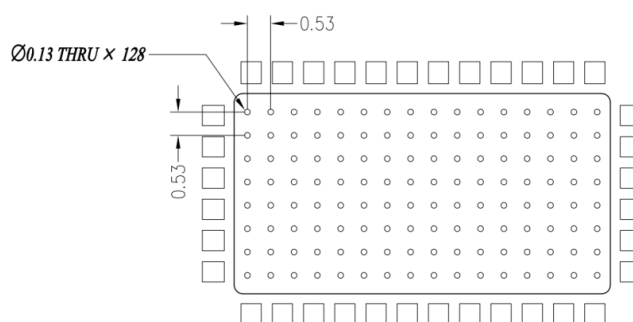
### 10\*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are  $\pm 0.2\text{mm}$ .

## Mounting Footprint Pattern



Notes:

1. All dimensions are in mm;
2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. ALL vias are PTH to ground.



## Revision history

Table 6. Document revision history

| Date      | Revision | Datasheet Status                                |
|-----------|----------|-------------------------------------------------|
| 2023/5/11 | Rev 1.0  | Preliminary Datasheet Creation                  |
| 2025/5/16 | Rev 2.0  | Modify the PCB layout by split of Vgs1 and Vgs2 |
|           |          |                                                 |

Application data based on ZHH-23-07/25-05

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