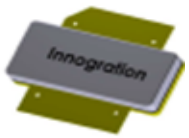
MC1065RVS LDMOS TRANSISTORs

Document Number: MC1065RVS
Preliminary Datasheet V1.1

650W, 0.5GHz 50V High Power RF LDMOS FETs

MC1065RVS



Description

The MC1065RVS is a 650watt capable, high performance, unmatched single ended and earless LDMOS FET, used for any frequency up to 0.5GHz,capable of delivery either CW or pulsed signal.

It is featured with high breakdown voltage and stability, and leading RF performance.

- Typical performance(on 325MHz narrow band application board with devices soldered)

V_{DS}=50V,I_{DQ}=50mA, CW

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	IDS(A)	Gain(dB)	Eff(%)
325	38.7	57.38	547.0	15.64	18.68	70.0
	39.63	57.75	595.7	16.6	18.12	71.8
	40.6	58	631.0	17.32	17.4	72.9
	41.46	58.2	660.7	17.94	16.74	73.7

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 85°C, 800W CW, 50 Vdc, I_{DQ} = 240 mA	Rth	0.24	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0V, I_{DS}=1.0mA	$V_{(BR)DSS}$		115		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	V_{GS}(th)	——	2.54	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 50 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.14	——	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured	Rds(on)		36		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		330		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		125		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		3.6		pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 50 mA, f = 325MHz, pulse width:100us, duty cycle:10%

10:1 at 650W Pulsed CW Output Power	No Device Degradation

Reference Circuit of Test Fixture (325MHz CW Power Amplifier)

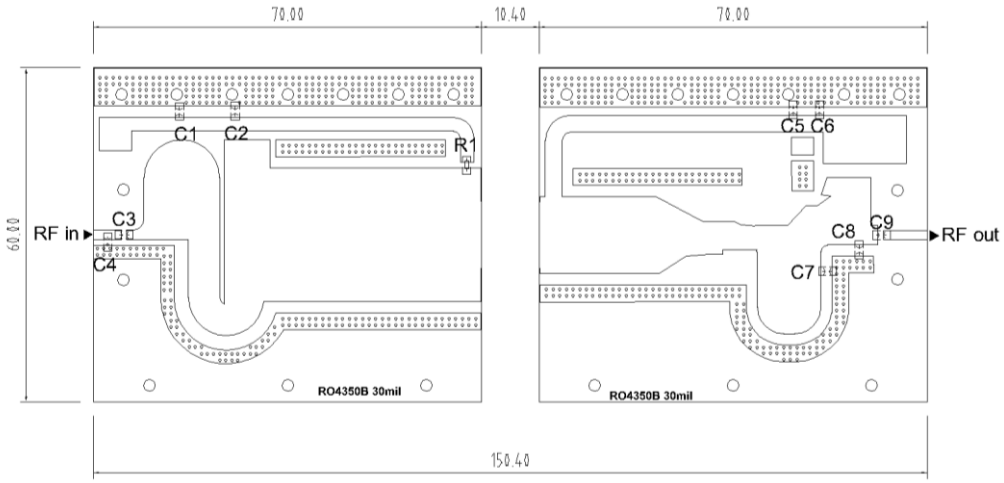
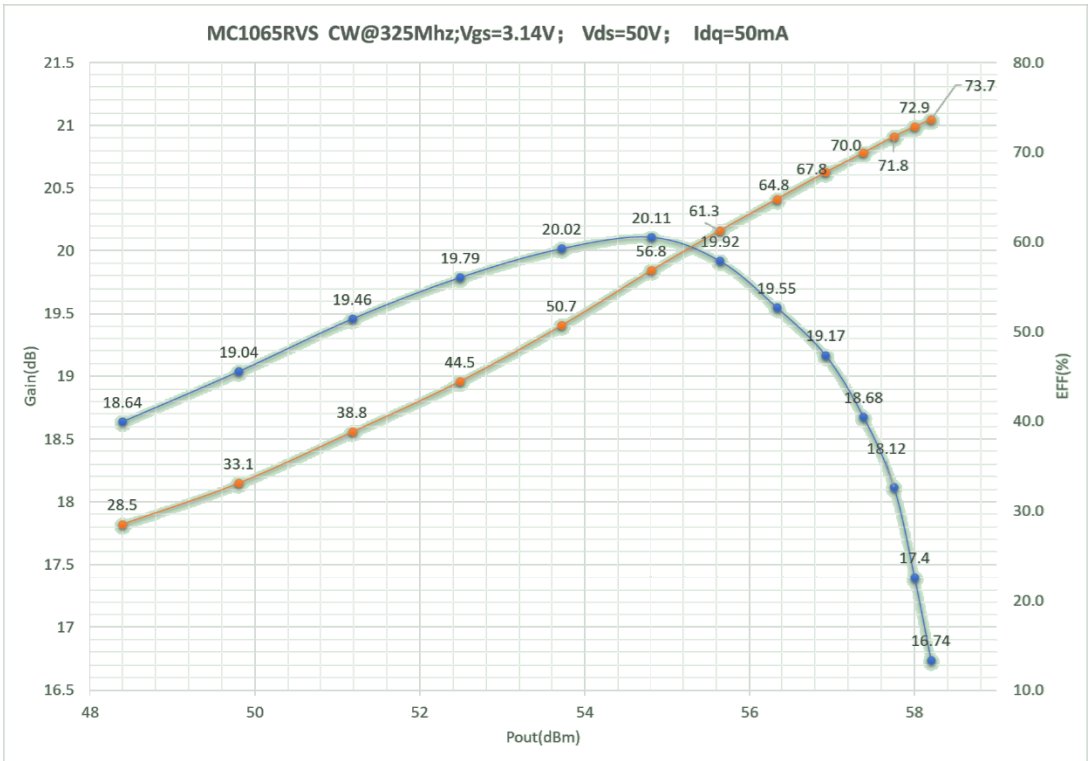


Table 5. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C2、C3、C5	150pF	ATC800B
C9	100pF*3	ATC800B
C1、C6	Ceramic multilayer capacitor, 10uF	
C4	30pF	ATC800B
C7	3.3pF	ATC800B
C8	30pF	ATC700C
R1	Chip Resistor,9.1Ω,1206	
PCB	30mil thickness,Ro4350B	

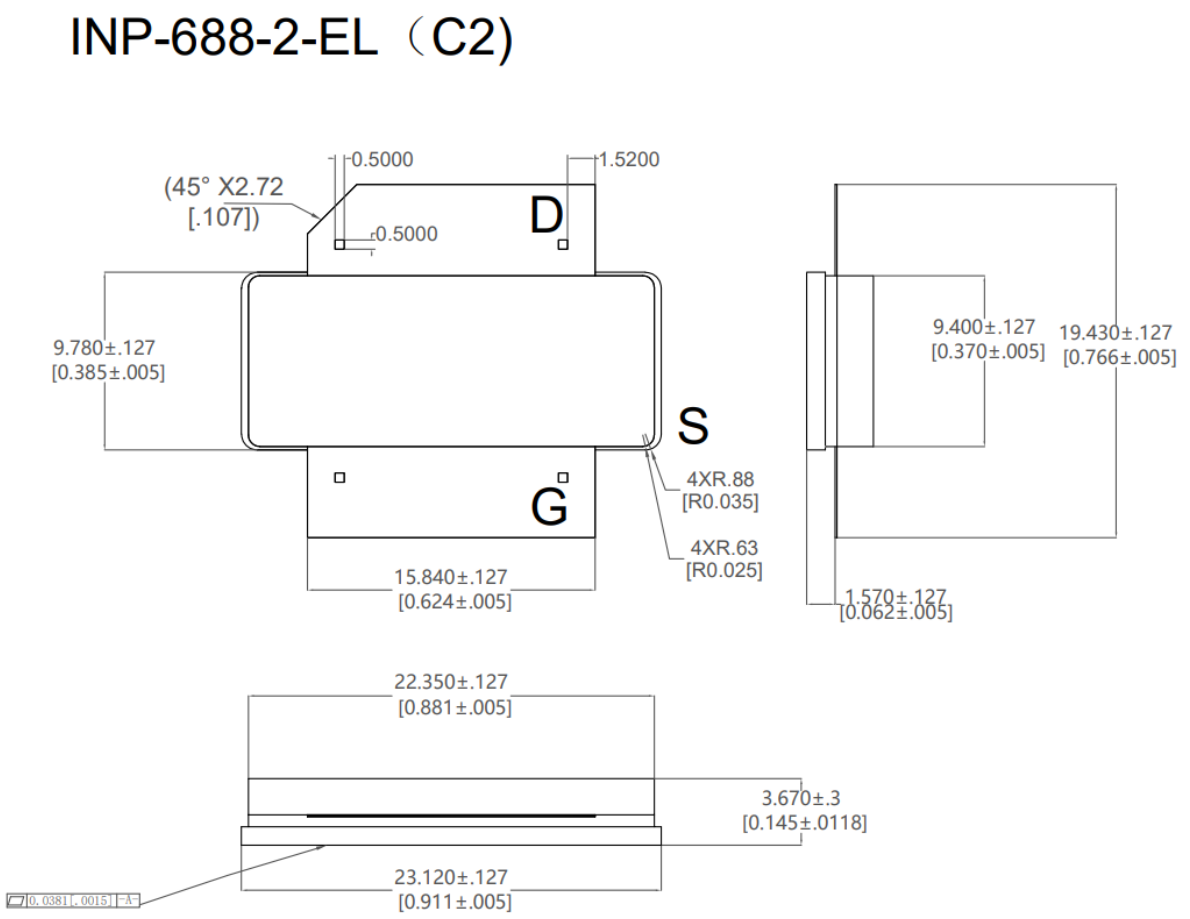
TYPICAL CHARACTERISTICS

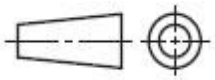
Figure 1: Pulsed CW Gain and Power Efficiency as a Function of Pout @100MHz at 50V



Package Outline

Flangeless ceramic package;



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/10/11	Rev 1.0	Preliminary datasheet
2023/5/14	Rev 1.1	Modify C9 as 3 pcs capacitors in parallel for power handling

Application data based on JF-21-15

Disclaimers