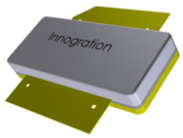
MC3515S LDMOS TRANSISTOR

Document Number: MC3515S
Product Datasheet V1.1

150W, S band High Power RF LDMOS FETs

MC3515S



Description

The MC3515S is a 150watt, internally matched, single ended LDMOS FETs, designed for S band commercial application within 2700-3500MHz full band. It can be used in Class AB/B and Class C for any pulse CW signal

•Typical Performance (On Innogration fixture with device soldered):

MC3515S VDS=28V Idq=200mA Vgs=2.5V Pulse 10% 100us						
F(MHz)	Pin（dBm）	Psat（dBm）	Psat（W）	I(A)	Gain（dB）	Eff(%)
2700	43	52.00	158	1.81	9.0	35.2
2800	42.1	52.00	158	1.74	9.9	36.8
2900	42.7	52.00	158	1.74	9.3	36.8
3000	43.5	52.00	158	1.75	8.5	36.5
3100	44	52.00	158	1.74	8.0	36.8
3200	43.8	52.00	158	1.64	8.2	39.3
3300	42.6	52.00	158	1.46	9.4	44.9
3400	42.8	52.00	158	1.44	9.2	45.6
3500	42.8	52.00	158	1.52	9.2	42.9

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- S band pulse CW amplifier
- ISM applications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class

Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65V, V_{GS} = 0 V)	I_{DSS}			100	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}			1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 450 μA)	$V_{GS(th)}$		1.9		V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$		2.4		V

Figure 1. Test Circuit Component Layout

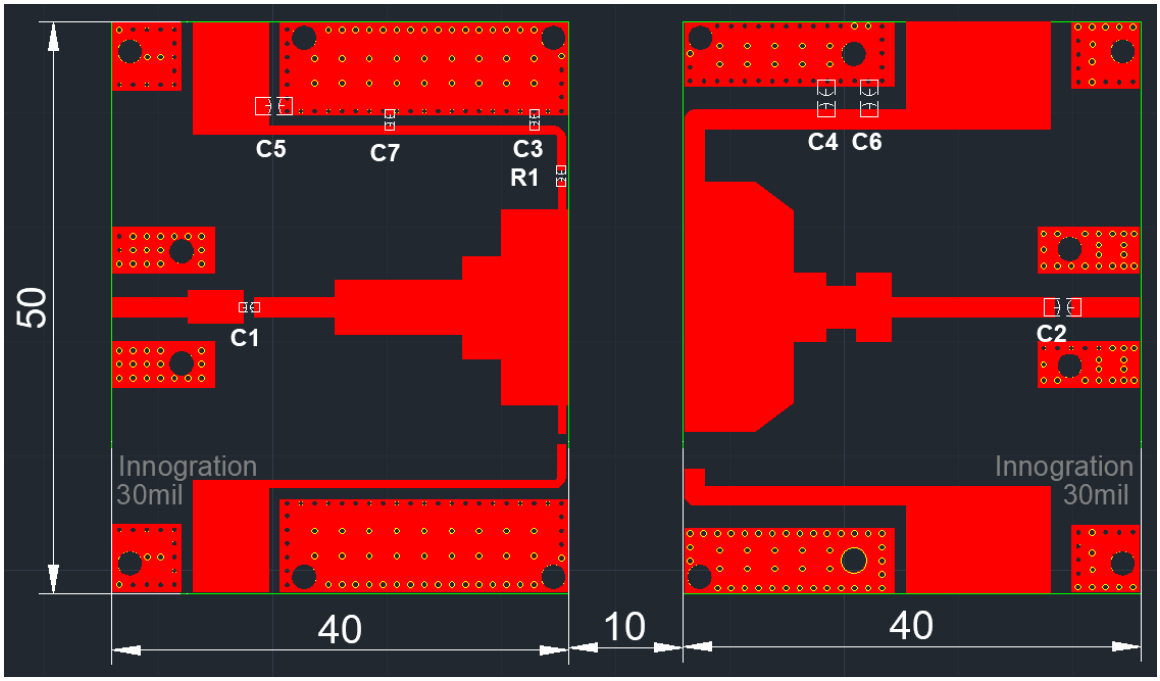


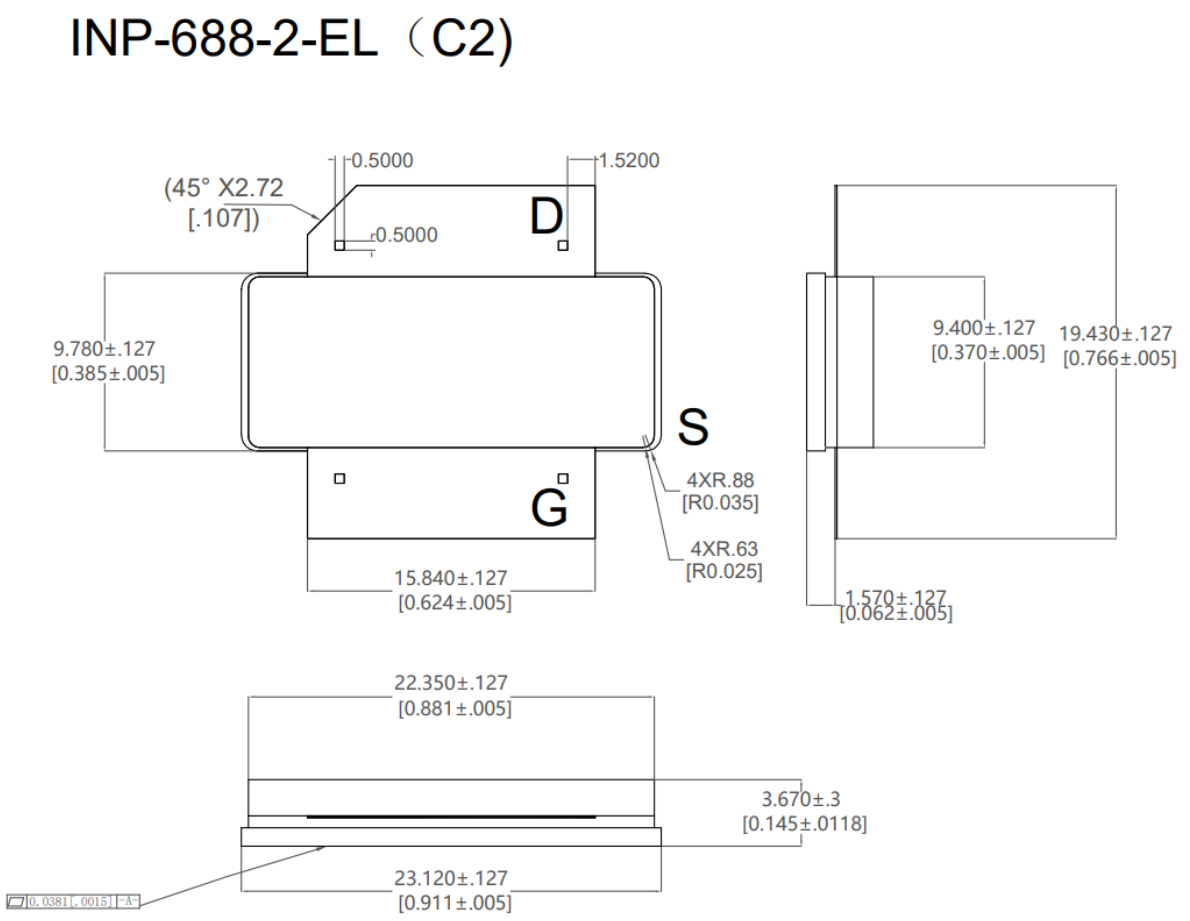
Table 4. Test Circuit Component Designations and Values

Part	description	Model
R1	7.50Ω	Chip Resistor
C1 ,C3	10pF 600F	
C2	15pF ATC 800R	
C4	12pF MQ10111	

C7	0.5PF MQ10111	
C5,C6	10uF 1210	
PCB	20mil Rogers4350B	

Package Outline

Flangeless ceramic package;



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/5/24	Rev 1.0	Product Datasheet Creation

Application data based on SXY-23-20

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