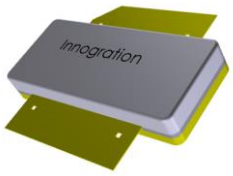
1400-1600MHz, 350W, 28V High Power RF LDMOS FETs

Description

The ITCH17351C2 is a 350-watt, internally matched LDMOS FETs, designed for multiple applications with frequencies from 1400 to 1600 MHz.

It Can be used in Class AB/B and Class C for all typical modulation formats.

ITCH17351C2



•Typical Performance (on test board with devices soldered):

V_{DS}=28V,I_{DQ}=330mA, CW

Freq(MHz)	Pin(dBm)	Pout(W)	IdsA)	Gain(dB)	Eff(%)
1475	39.9	325.1	20.35	15.22	57.1%
1500	39.8	316.2	19.6	15.2	57.6%
1525	39.8	316.2	19.7	15.2	57.3%

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Optimized for Doherty Applications
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	70	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 350W Pulsed Output	$R_{\theta JC}$	0.22	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage	V_{DSS}	65	——	——	V

(V_{GS}=0V; I_D=100uA)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 uA)	$V_{GS(th)}$	——	1.6	——	V
Gate Quiescent Voltage (V_{DS} = 28 V, I_{DQ} = 350 mA, Measured in Functional Test)	$V_{GS(Q)}$	2.1	2.6	3.1	V

Functional Tests (In Innogration Test Fixture, 50 ohm system) :V_{DS} = 28 Vdc, I_{DQ} = 350 mA, f = 1400 MHz, Pulse CW Signal Measurements.

(Pulse Width=20 μs, Duty cycle=10%)

Power Gain @ P_{1dB}	Gp	——	17	——	dB
Drain Efficiency@P3dB	η_D	——	57	——	%
3dB Compression Point	P_{-3dB}	——	55	——	dBm
Input Return Loss	IRL	——	-7	——	dB

Load Mismatch of per Section (On Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 350 mA, f = 1400 MHz

VSWR 5:1 at 350W pulse CW Output Power	No Device Degradation

Reference Circuit of Test Fixture Assembly Diagram

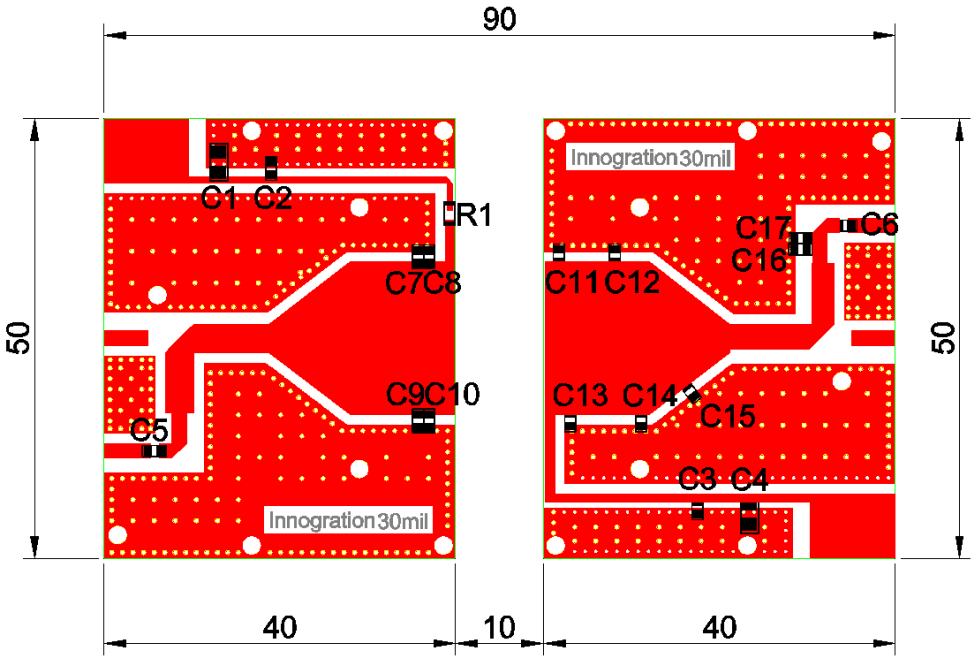


Figure 1. Test Circuit Component Layout (1475-1525MHz)

Table 1. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C2、C3、C5、	39pF	DLC70B
C6	10pF*4	DLC70B
C1、C4、	10uF/50V	1210
C7、C9	1.0pF	DLC70B
C8、C10	2.7pF	DLC70B
C11、C13	4.7pF	DLC70B
C12、C14、C15	1.5pF	DLC70B
C16、C17	0.5pF	DLC70B
R1	Chip Resistor,9.1Ω,1206	
PCB	30Mil Rogers 4350B	

TYPICAL CHARACTERISTICS

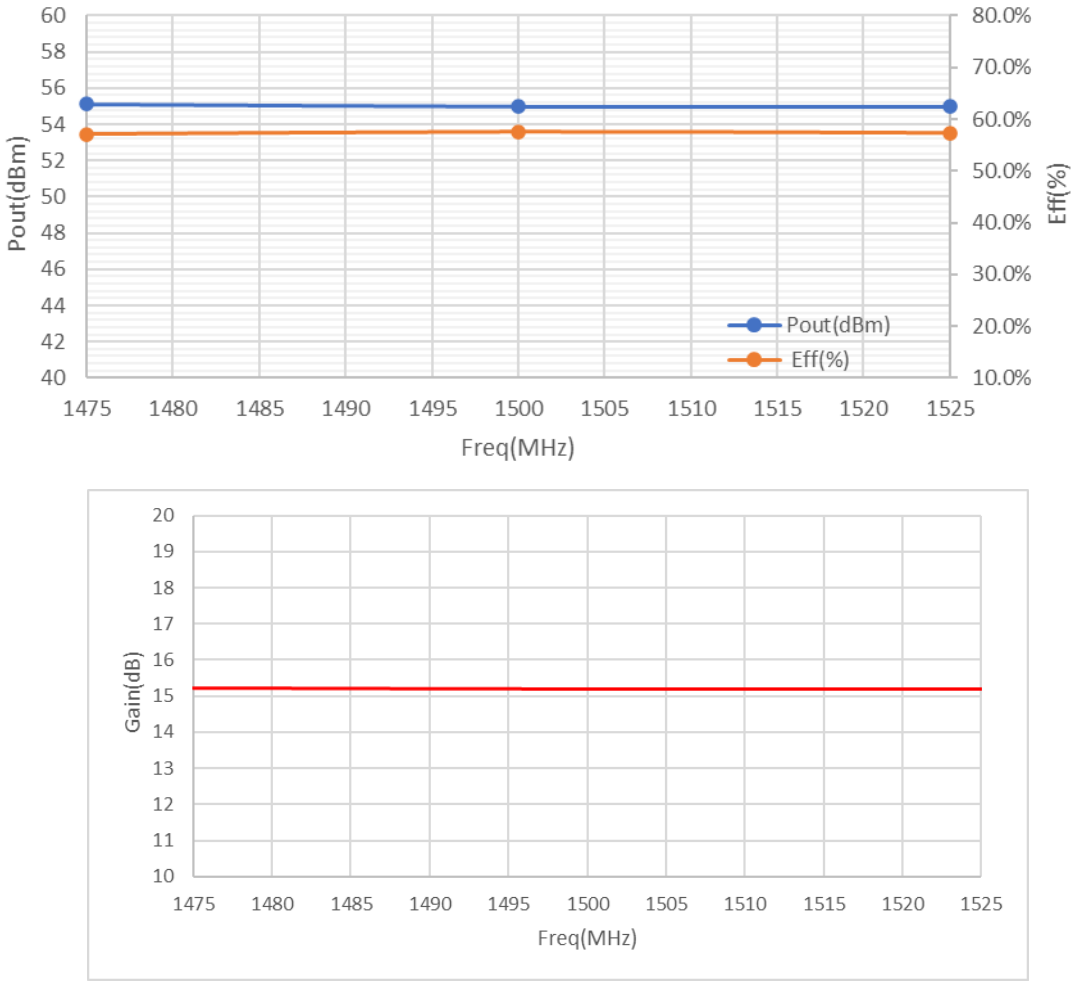


Figure 2. Power Gain and Drain Efficiency as Function of CW Output Power

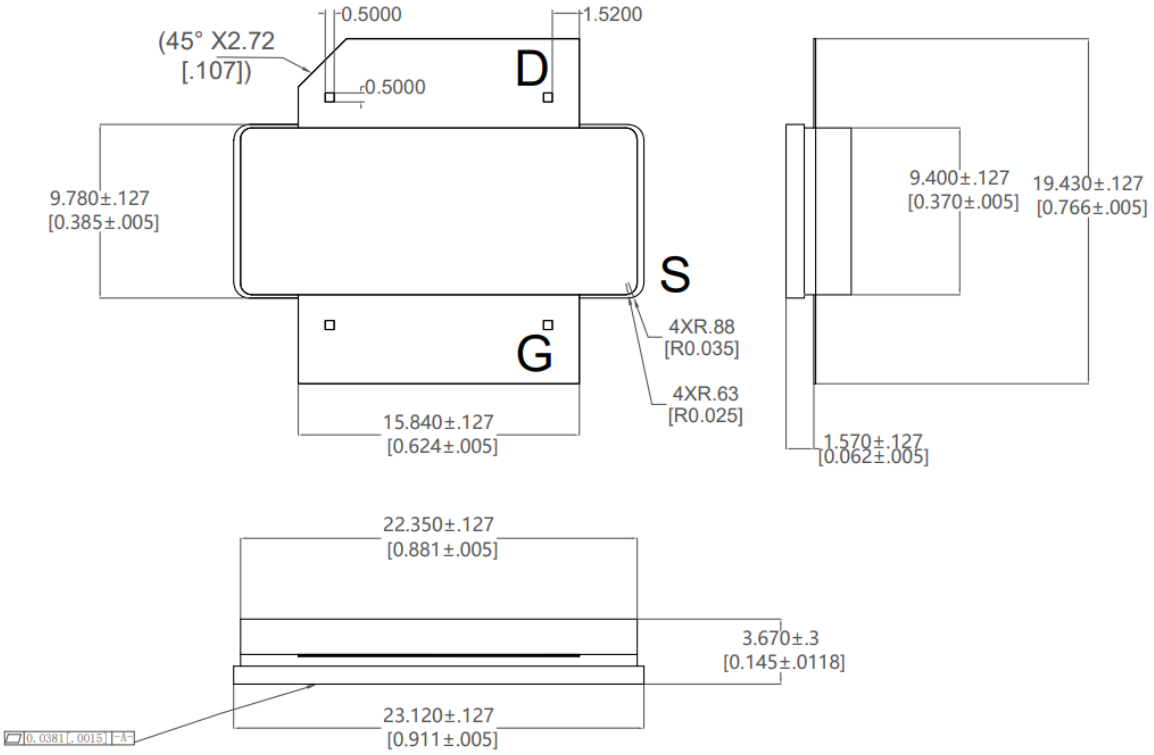
Figure 3. Network analyzer output S11/S21

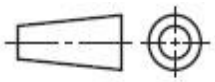
Vgs=2.73V Vds=28V,Idq =1A

Package Outline

Flangeless ceramic package;

INP-688-2-EL（C2)



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2022/8/8	V1.0	Preliminary Datasheet Creation
2023/5/26	V1.1	Modify C6 to multiple smaller caps for power handling
2025/8/28	V1.2	Correct C2 drawing

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