



GaN HEMT 50V, 500W, 2.3-2.4GHz RF Power Transistor

Description

The STBV24500BY4 is a dual path 500watt , Input matched GaN HEMT, ideal for applications from 2.3 to 2.4GHz especially for LTE/5G. In typical 8.5-9.5dB back off condition, it can deliver 55 to 70W linearizable average power

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical RF performance on asymmetrical Doherty with device soldered

VDS= 50V, IDQ=200mA(Vgm=-3.2V, Vgp=-5.10V)

WCDMA 1 carrier performance

Freq (MHz)	Pout (dBm)	CCDF (dB)	Ppeak (dBm)	Ppeak (W)	ACPR (dBc)	Gain (dB)	Efficiency (%)
2300	48.48	8.53	57.01	502.6	-28.4	16.4	56.9
2350	48.49	8.53	57.02	503.0	-30.2	15.9	57.1
2400	48.49	8.14	56.63	460.1	-32.8	15.4	55.8

Recommended driver: Class AB (1 stage discrete solution): STAV38041C6

Applications

- Asymmetrical Doherty amplifier within 2.3-2.4GHz
- S band power amplifier
- CW or pulsed Amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

STBV24500BY4

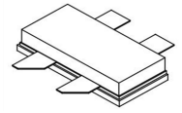


Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

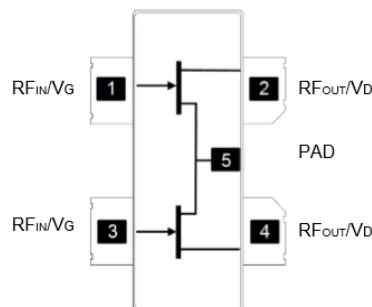


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+200	Vdc
Gate--Source Voltage	V _{GS}	-8 to +0.5	Vdc
Operating Voltage	V _{DD}	55	Vdc



Maximum gate current	I _{gs}	65	mA
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _C	+150	°C
Operating Junction Temperature	T _J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T _C = 85°C, at Pd=50W, on Doherty application board	R _{θJC}	1	°C /W

Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics (Main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{GS} =-8V; I _{DS} =25.2mA	V _{DSS}		200		V
Gate Threshold Voltage	V _{DS} =10V, I _D = 25.2mA	V _{GS(th)}	-4		-2	V
Gate Quiescent Voltage	V _{DS} =50V, I _{DS} =150mA, Measured in Functional Test	V _{GS(Q)}		-3.07		V

DC Characteristics (Peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{GS} =-8V; I _{DS} =39.6mA	V _{DSS}		200		V
Gate Threshold Voltage	V _{DS} =10V, I _D = 39.6mA	V _{GS(th)}	-4		-2	V
Gate Quiescent Voltage	V _{DS} =50V, I _{DS} =150mA, Measured in Functional Test	V _{GS(Q)}		-3.0		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.35GHz, P _{out} =55W WCDMA 1 Carrier in Doherty circuit All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature

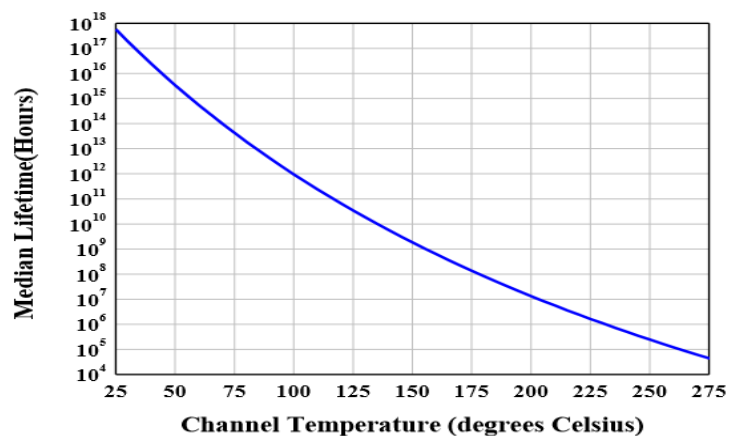
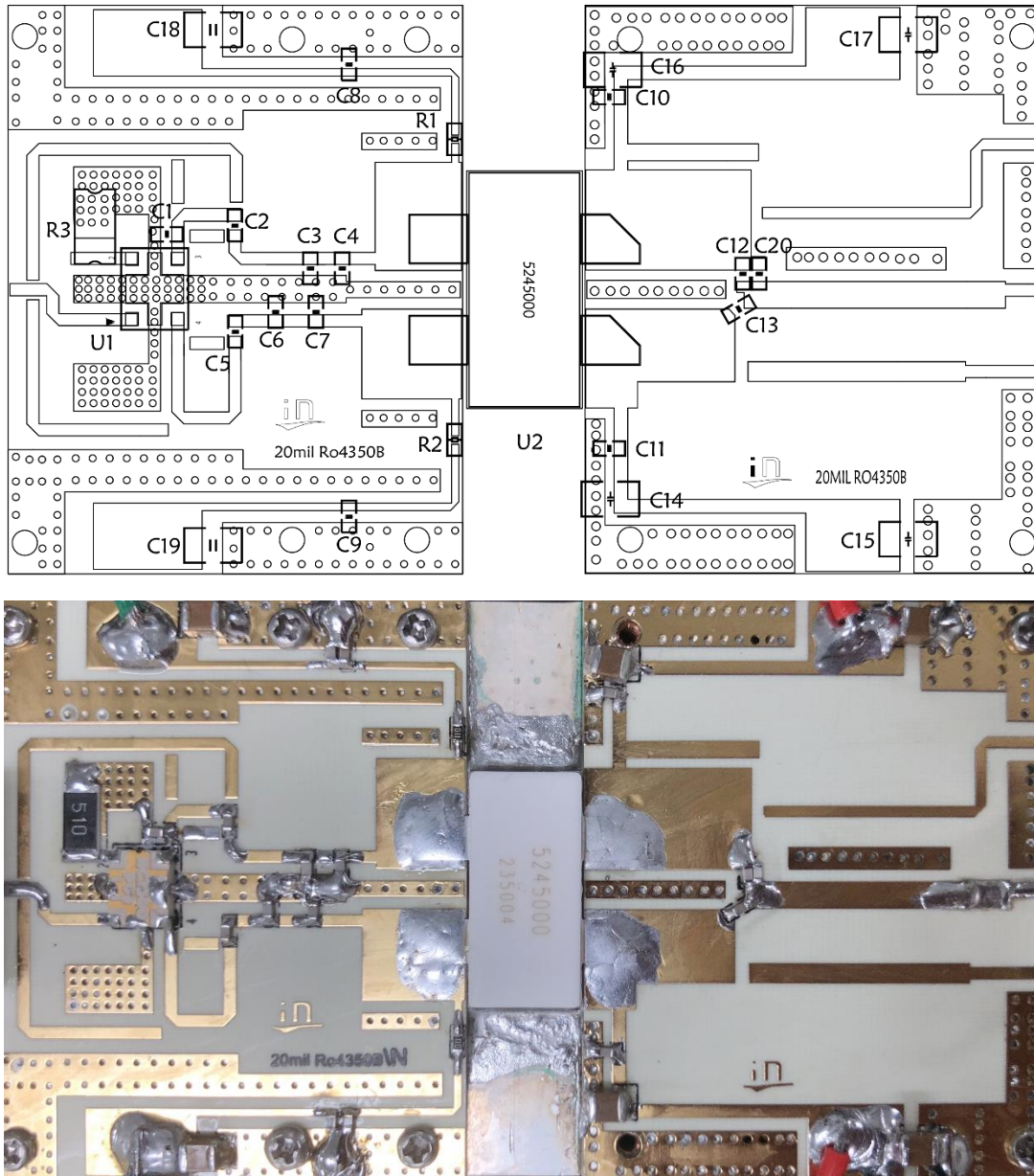


Figure 3: Picture of application board Doherty circuit for 2.3-2.4GHz



Reference	Footprint	Value	Quantity
C1	0603	0.4pF/250V	1
C2, C13	0603	10pF/250V	2
C3	0603	2.0pF/250V	1
C4, C6, C7	0603	1.1pF/250V	3
C5, C8, C9, C10, C11	0603	20pF/250V	5
C12	0603	1.6pF/250V	1
C20	0603	0.1pF/250V	1
C14, C15, C16, C17, C18, C19	1210	10uF/100V	6
R1, R2	0603	10R	2



R3	2512	51R	1
U1	6.35*5.08mm	HC2500P03	1
U2	BY4	5245000	1

Figure 3: Efficiency and power gain as function of Pout

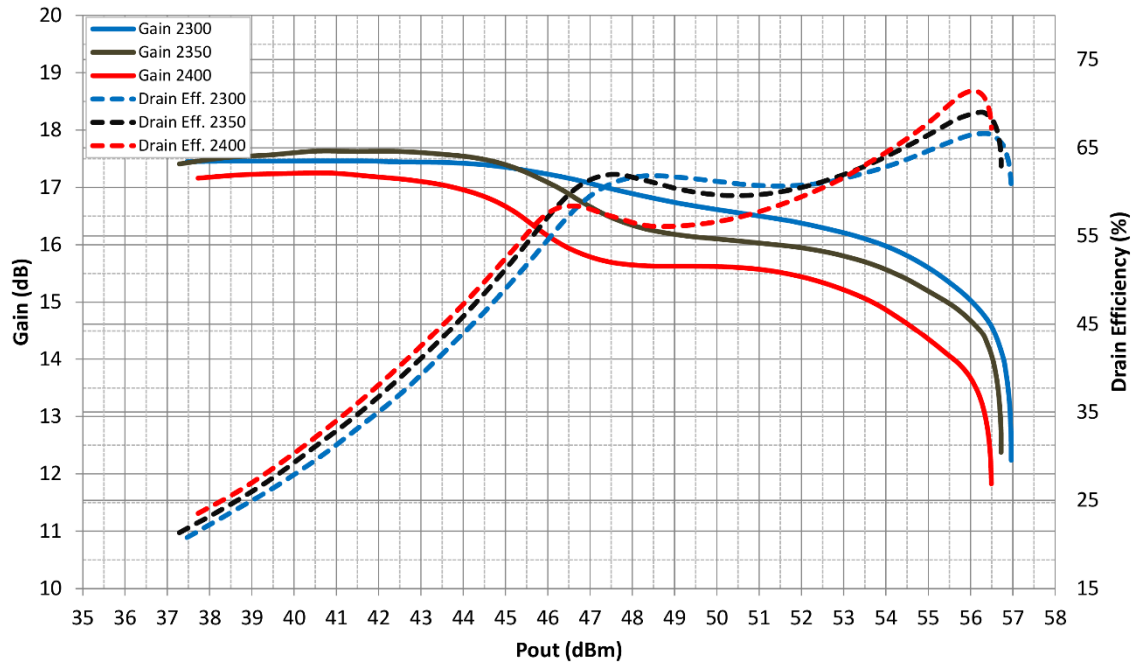
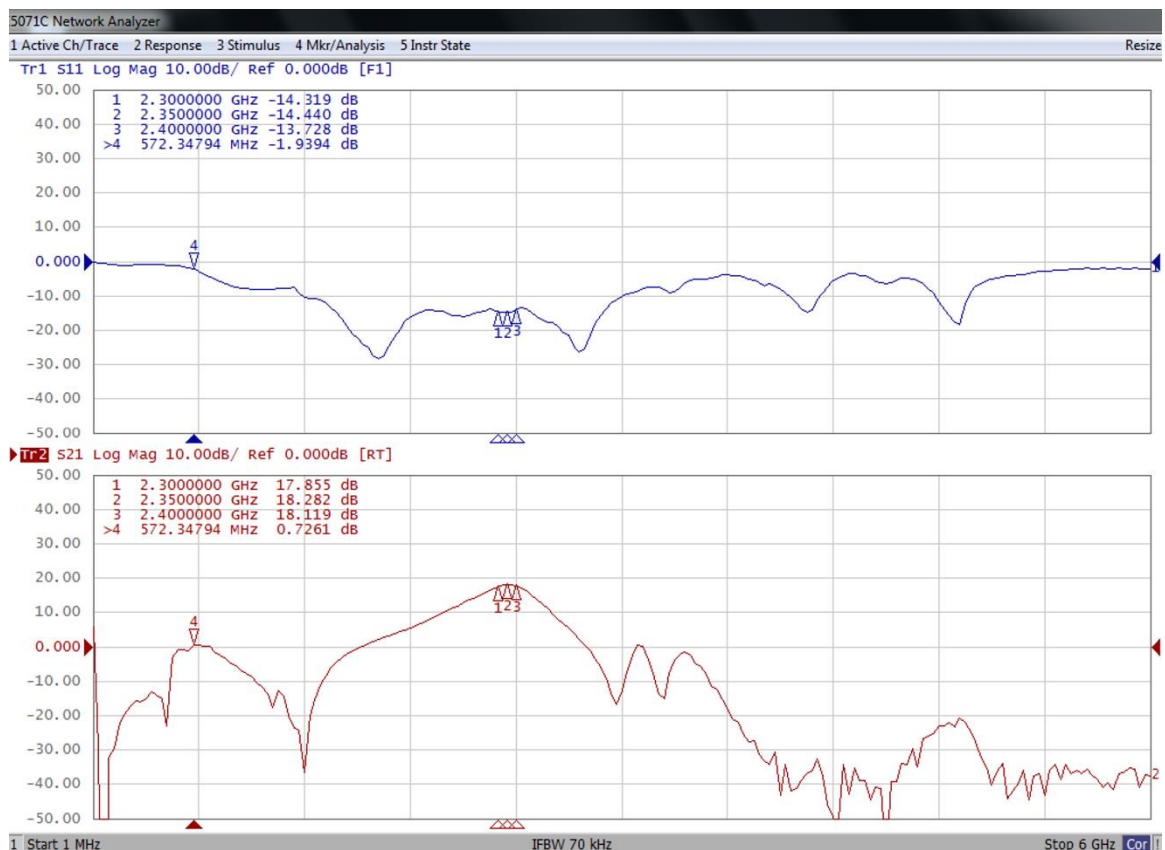
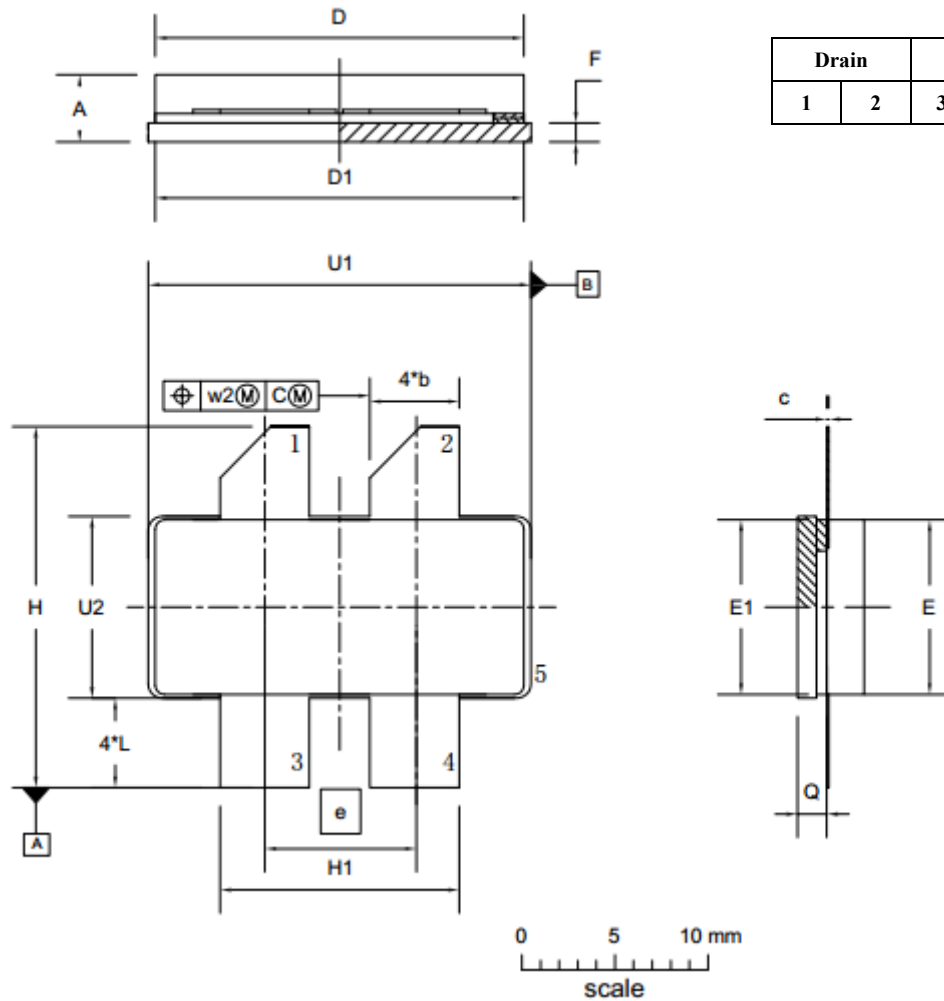


Figure 5: Network analyzer output, S11 and S21





Earless Flanged Ceramic Package; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₁	W ₂
mm	4.72	4.67	0.15	20.02	19.96	7.90	9.50	9.53	1.14	19.94	12.98	5.33	1.70	20.70	9.91	0.25	0.51
	3.43	4.93	0.08	19.61	19.66		9.30	9.25	0.89	18.92	12.73	4.32	1.45	20.45	9.65		
inches	0.186	0.194	0.006	0.788	0.786	0.311	0.374	0.375	0.045	0.785	0.511	0.210	0.067	0.815	0.390	0.01	0.02
	0.135	0.184	0.003	0.772	0.774		0.366	0.364	0.035	0.745	0.501	0.170	0.057	0.805	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/5/16	V1.0	Objective Datasheet Creation
2023/5/30	V1.0	Preliminary Datasheet Creation
2025/1/11	V1.1	Update according to latest application result

Application data based on ZBB-25-03

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