



GaN 50V,480W, RF Power Transistor

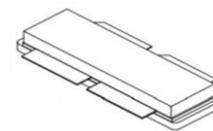
Description

The SQ3048RVPS is a push pull 480W capable, internally matched GaN HEMT, ideal for multiple applications up to 3GHz. It is optimized thermally to support higher duty cycle or longer pulse up to CW application.

In typical wideband application from 700 to 910MHz, it can deliver 400W across the full band.

There is no guarantee of performance when this part is used outside of stated frequencies.

SQ3048RVPS



- Typical Pulsed CW performance at 700-910MHz applications

SQ3048RVPS ^{V0} V _{DS} =50V V _{GS} =-3.24V I _{DQ} =200mA Pulse width 12us 50%								
Freq (MHz)	Psat (dBm)	Psat (W)	IDS (A)	Pin (dBm)	Gain (dB)	Eff(%)	2 nd Harmonic(dBc)	3 rd Harmonic(dBc)
700	56.8	478.63	6.96	39.45	17.35	68.77	-22.6	-21.8
750	56.65	462.38	7.05	36.94	19.71	65.59	-21.9	-26.4
800	56.86	485.29	6.91	37.81	19.05	70.23	-20.5	-30.4
850	56.99	500.03	7.60	37.78	19.21	65.79	-25.1	-41.9
900	56.25	421.70	6.47	37.08	19.17	65.18	-19.6	-55.8
910	56.8	478.63	6.96	39.45	17.35	68.77	-22.6	-21.8

CW data upon request

Applications

- P band power amplifier
- UHF TV
- Public Safety Radio
- Data link power amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch-off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+200	Vdc
Gate--Source Voltage	V _{GS}	-8 to +0.5	Vdc
Operating Voltage	V _{DD}	55	Vdc



Maximum gate current	I _{gs}	60	mA
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T _c = 25°C, at P _{out} =400W @900MHz	R _{θJC}	0.31	°C /W

Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

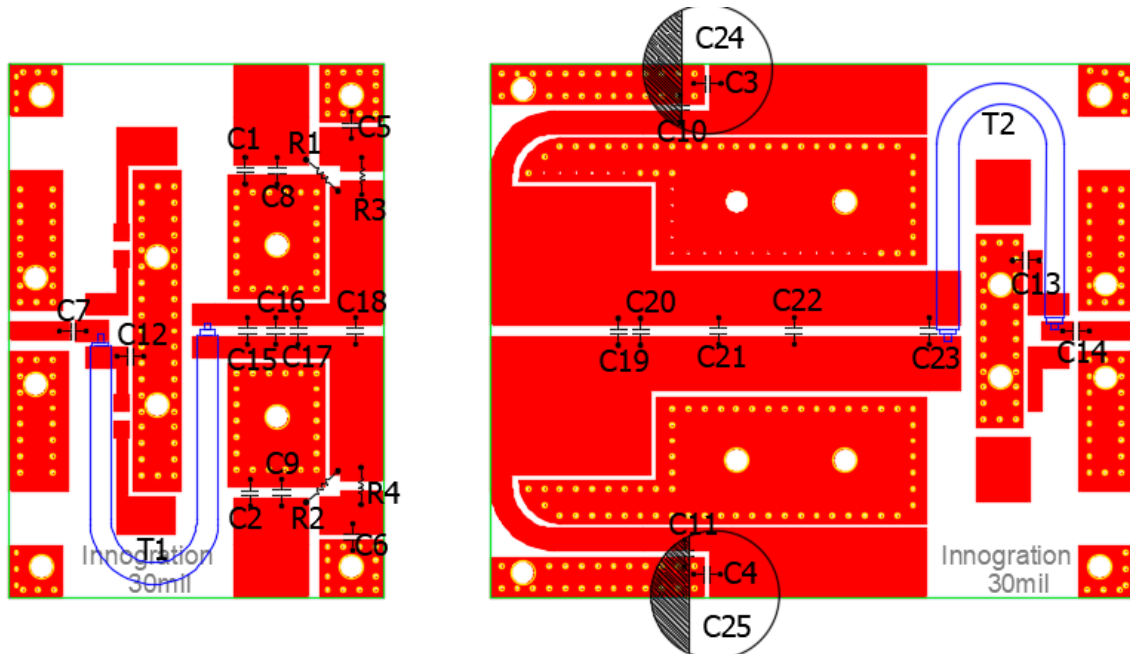
DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{GS} =-8V; I _{DS} =60mA	V _{DSS}		200		V
Gate Threshold Voltage	V _{DS} =10V, I _D = 60mA	V _{GS(th)}	-4	-	-2	V
Gate Quiescent Voltage	V _{DS} =50V, I _{DS} =180mA, Measured in Functional Test	V _{GS(Q)}		-3.2		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	900MHz, P _{out} =400W pulse CW All phase, No device damages	VSWR		5:1		

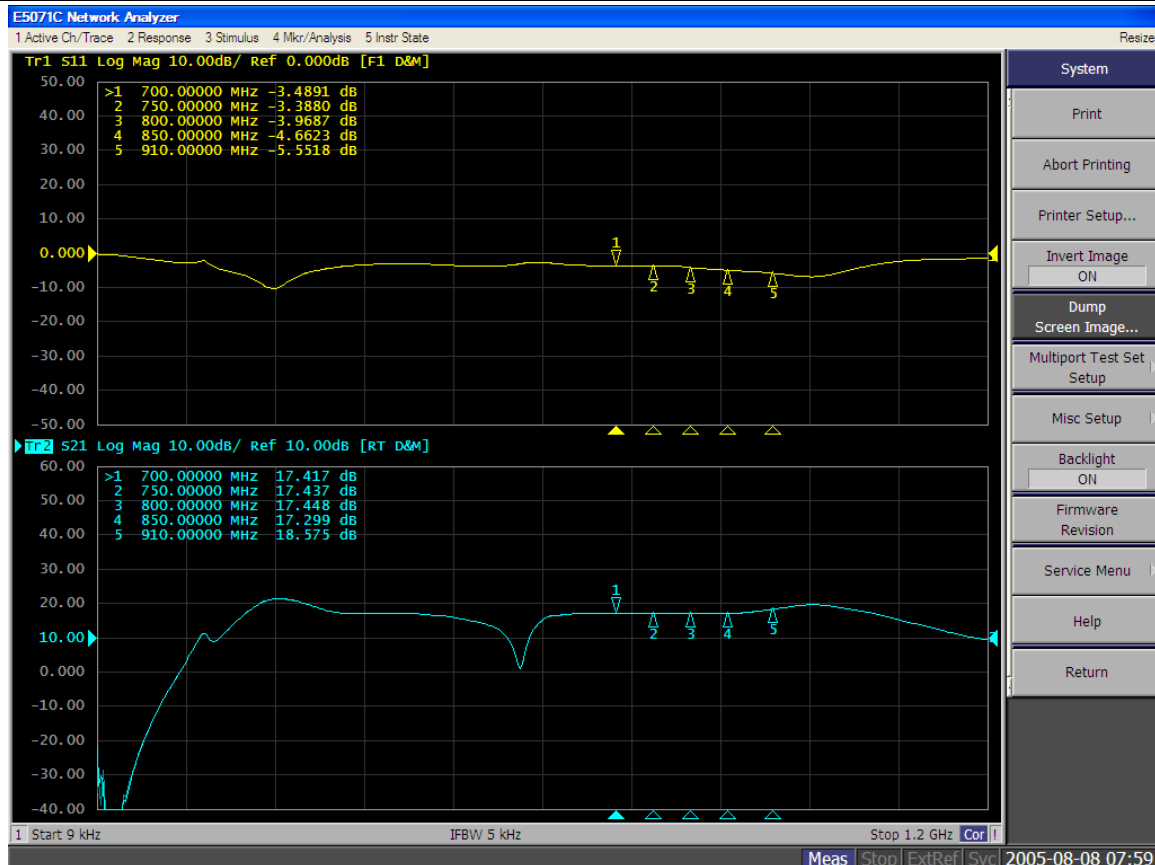
Figure 1: Reference design circuit (PCB DWG file upon request,)



Component	Description	Suggestion
C1~C4	10uF/1210	Ceramic Multilayer Capacitor
C5,C6	1000pF	BEIJING YUANLU HONGYUAN ELECTRONIC TECHNOLOGY CO., LTD.MQ301111
C7	33pF	BEIJING YUANLU HONGYUAN ELECTRONIC



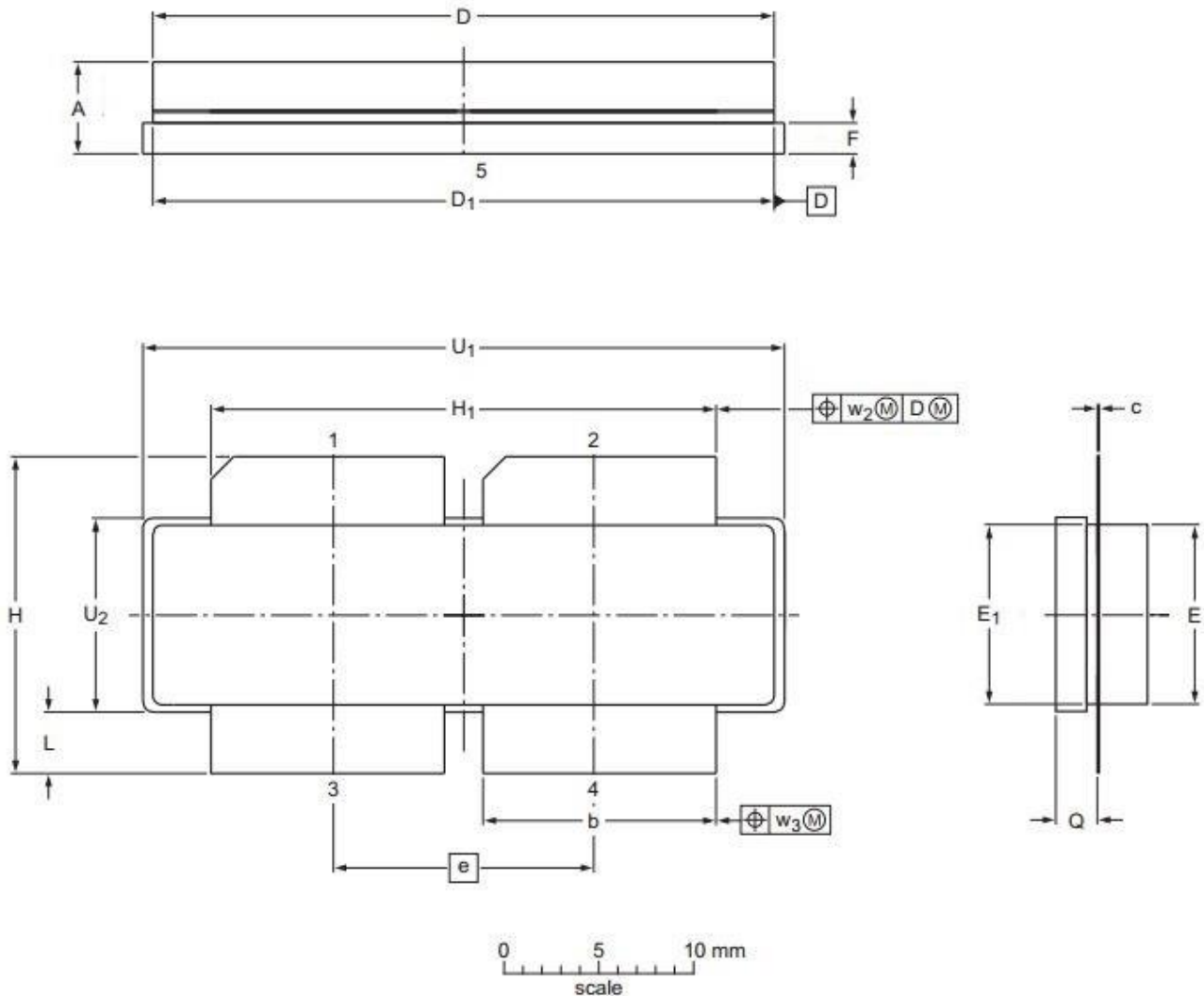
		TECHNOLOGY CO., LTD.MQ300805
C8~C14	33pF	BEIJING YUANLU HONGYUAN ELECTRONIC TECHNOLOGY CO., LTD.MQ301111
C15,C20	3pF	BEIJING YUANLU HONGYUAN ELECTRONIC TECHNOLOGY CO., LTD.MQ301111
C16,C18	6.8pF	BEIJING YUANLU HONGYUAN ELECTRONIC TECHNOLOGY CO., LTD.MQ301111
C17	10pF	BEIJING YUANLU HONGYUAN ELECTRONIC TECHNOLOGY CO., LTD.MQ301111
C19	1pF	BEIJING YUANLU HONGYUAN ELECTRONIC TECHNOLOGY CO., LTD.MQ301111
C21,C22	4.7pF	BEIJING YUANLU HONGYUAN ELECTRONIC TECHNOLOGY CO., LTD.MQ301111
C23	0.8pF	BEIJING YUANLU HONGYUAN ELECTRONIC TECHNOLOGY CO., LTD.MQ301111
C24,C25	2200uF/63V	Electrolytic capacitor
T1	25ohm 50mm	SFRFBU-086-50
T2	35ohm 50mm	SFXF-35-3
R1,R2	50 Ω	Pulg-in Resistor
R3,R4	18 Ω /1206	Chip Resistor
PCB	30Mil Rogers4350	





Package Outline

Earless flanged ceramic package; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₂	W ₂
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/5/5	V1.0	Preliminary Datasheet Creation
2025/3/11	V1.1	Update with improved application data

Application data based on: HL-23-15/25-10

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