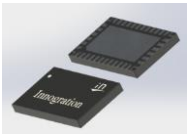
40W,28V Plastic RF LDMOS Transistor

ITEH38040C6



Description

The ITEH38040C6 is a 40-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies 3.3 to 3.8GHz, in 10*6mm QFN plastic package, supporting surface mounted on PCB through high density grounding vias.

•Typical Class AB RF Performance (On Innogration **3.3-3.6GHz f**ixture with device soldered).

VDS=**28V**, IDQ=300mA, 1 carrier WCDMA **high linearity tuning**

Freq (MHz)	Pout (dBm)	ACPR (dBc)	Gain (dB)	Efficiency (%)
3300	34	-46.5	13.9	10.6
3450	34	-47.4	13.8	10.9
3600	34	-47.0	13.7	11.3

•Typical Class AB RF Performance (On Innogration **3.6-3.8GHz** fixture with device soldered).

VDS=**28V**, IDQ=300mA, 1 carrier WCDMA **high linearity tuning**

Freq (MHz)	Pout (dBm)	ACPR (dBc)	Gain (dB)	Efficiency (%)
3600	34	-47.2	12.7	10.9
3700	34	-49.1	12.6	11.6
3800	34	-48.2	12.5	12.0

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- S band power amplifier
- All 4G/5G cellular application within 3.3 to 3.8GHz

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+28	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		65		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 11 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 μA)	$V_{GS}(th)$	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 28V, I_D = 350mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.7	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28Vdc, I_{DQ} = 350 mA, f = 3600 MHz

VSWR 10:1 at 40W pulse CW Output Power	No Device Degradation

Figure 1:Pin Definition(Top View)

Pin No.	Symbol	Description
8,9,10,11,14,15,16,17	Vgs/RF In	Vgs and RF input
26,27,28,29,32,33,34,35	Vds/RF out	Vds and RF output
2,5,7,12,13,18,20,23,25,30,31,36	GND	DC/RF Ground
Others	NC	No connection
Package Base	GND	DC/RF Ground.

3.3-3.6GHz application board

Reference Circuit of Test Fixture Assembly Diagram
20mils RO4350B

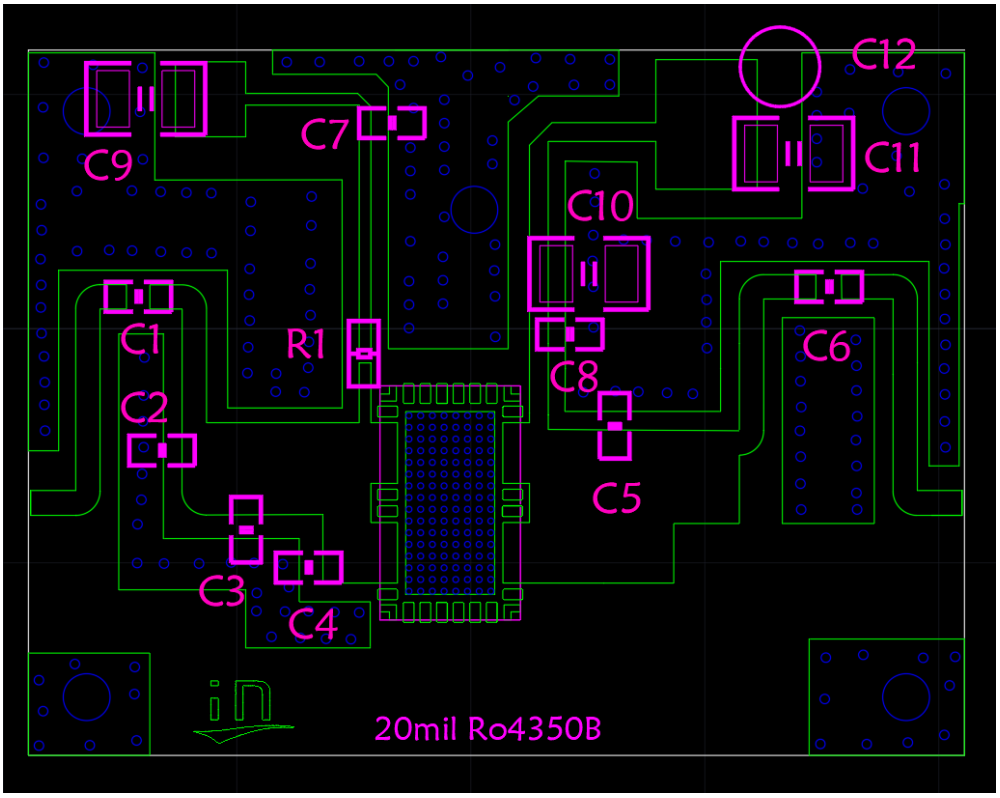


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Reference	Footprint	Value	Quantity
C1, C6, C7, C8	0603	8.2pF	4
C2	0603	0.3pF	1
C3, C5	0603	0.5pF	2
C4	0603	1pF	1
C9, C10, C11	1210	10uF/63V	3
C12		470uF/63V	1
R1	0603	10Ω	1

TYPICAL CHARACTERISTICS

Figure 3. Power Gain and Drain Efficiency as function of Power Output

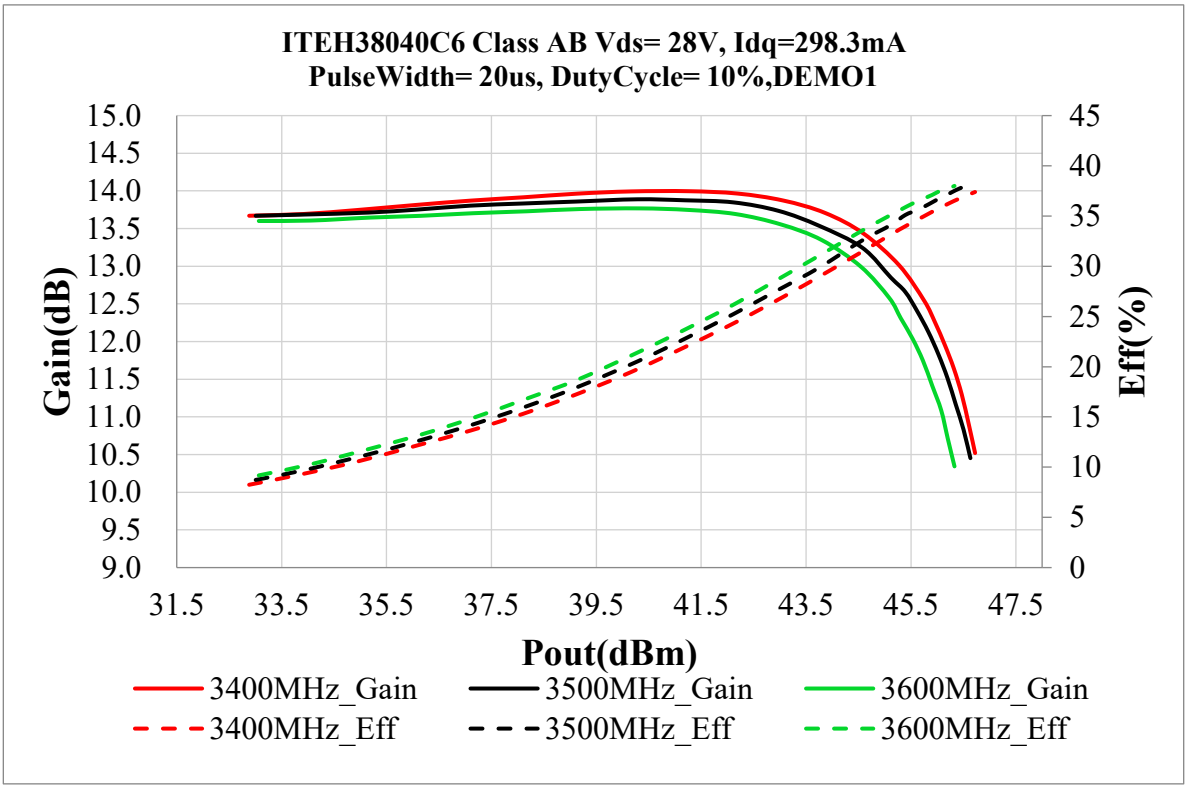
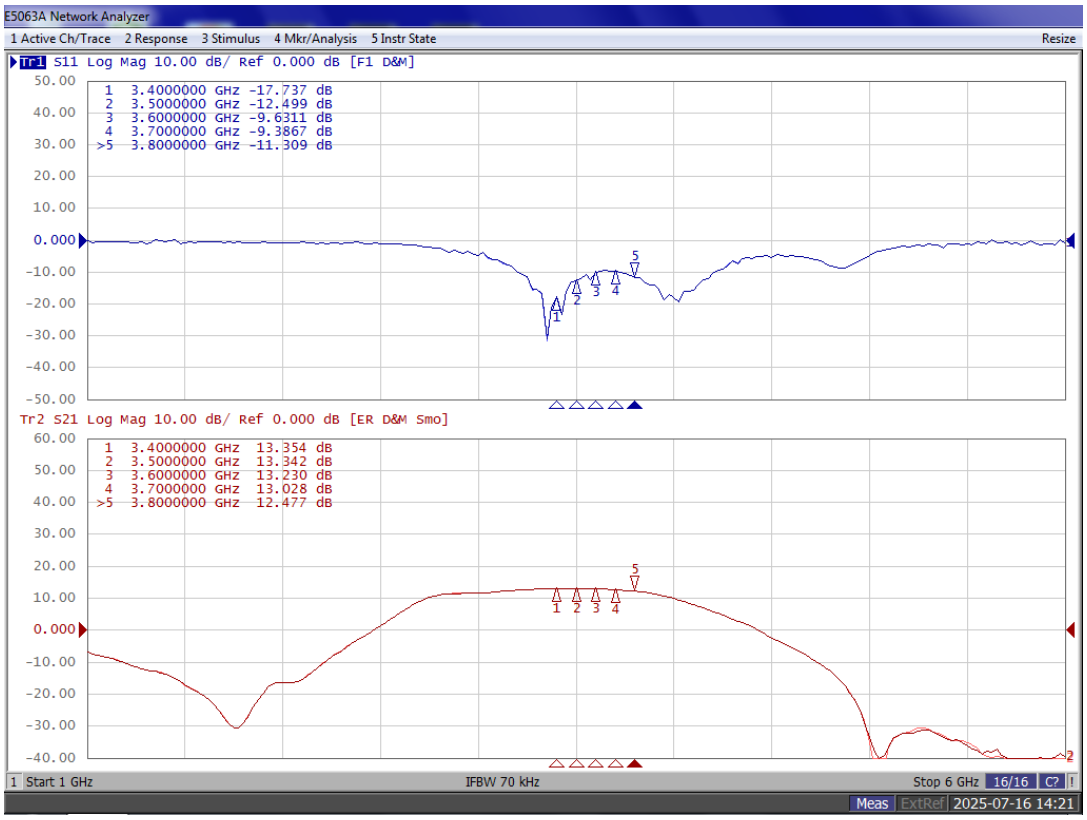


Figure 4.Network analyzer output S11/S21



3.6-3.8GHz application board

Reference Circuit of Test Fixture Assembly Diagram
20mils RO4350B

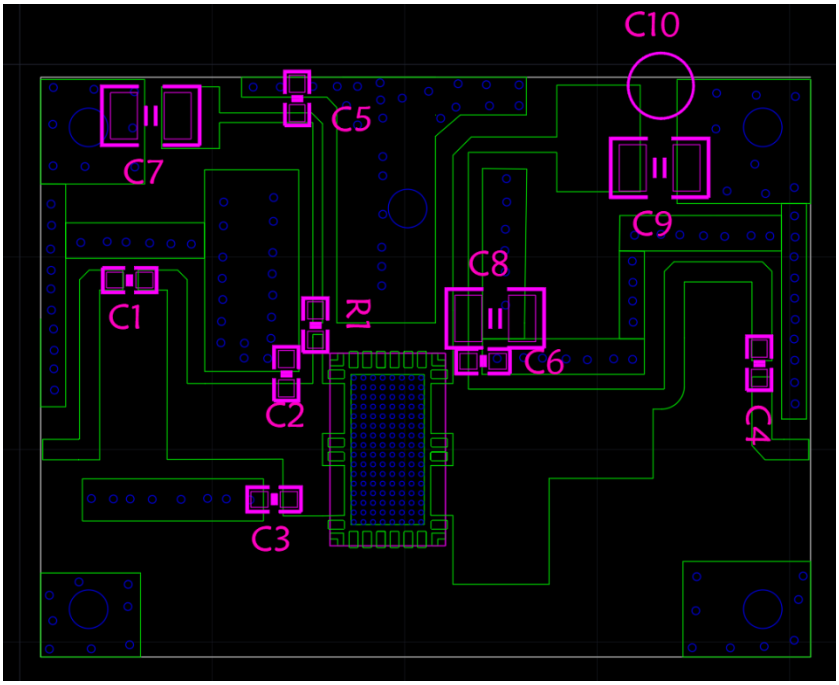


Figure 5. Test Circuit Component Layout

Table 6. Test Circuit Component Designations and Values

Reference	Footprint	Value	Quantity
C1, C4, C5, C6	0603	8.2pF	4
C3	0603	0.5pF	1
C2	0603	1pF	1
C7, C8, C9	1210	10uF/63V	3
C10		470uF/63V	1
R1	0603	10Ω	1

TYPICAL CHARACTERISTICS

Figure 7 . Power Gain and Drain Efficiency as function of Power Output

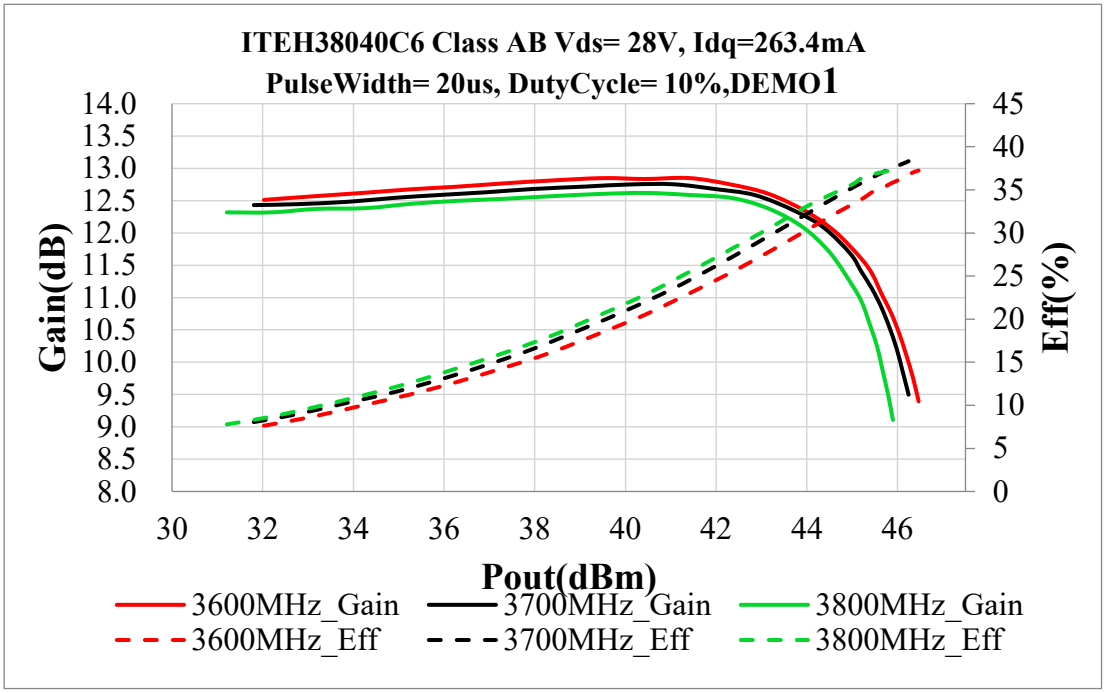
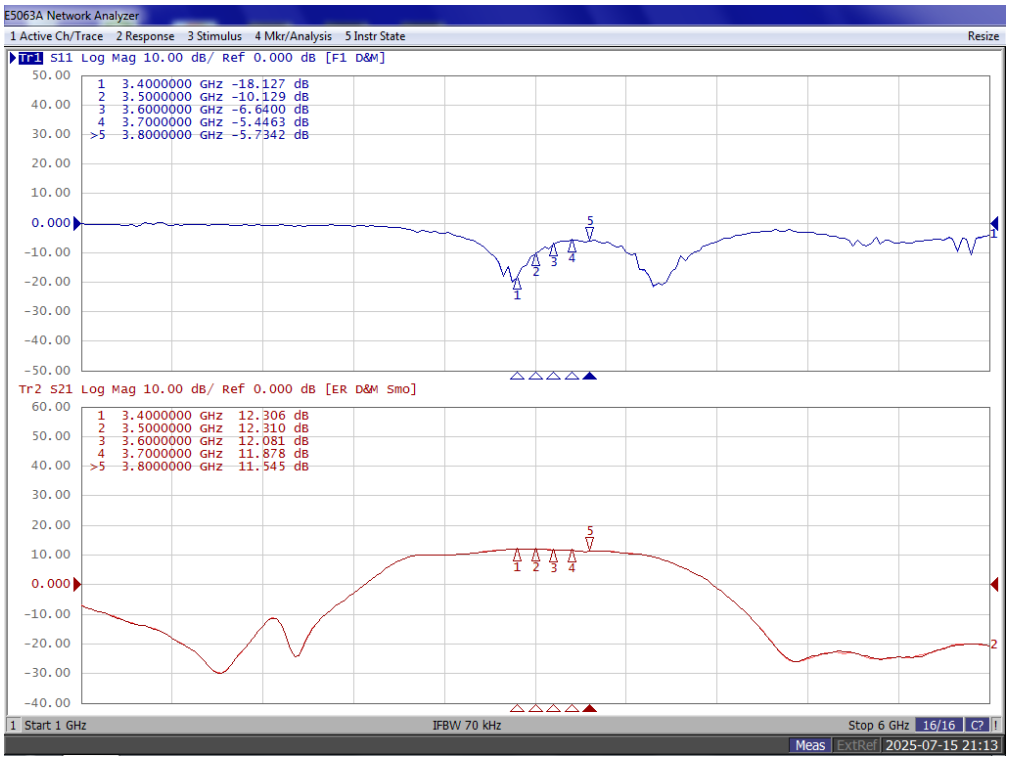
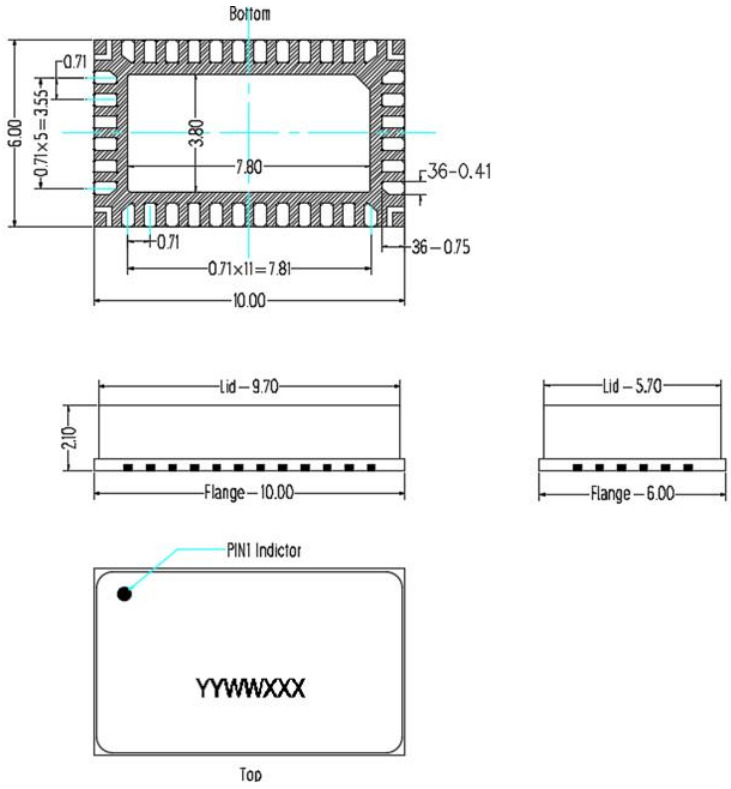


Figure 8 Network analyzer output S11/S21



Package Dimensions

10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.2mm.

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2023/3/30	**Rev 1.0**	**Preliminary Datasheet**
2023/5/10	**Rev 1.1**	Add 3.6-3.8GHz application data
2023/6/26	**Rev 1.2**	Update 3.3-3.6GHz application data for high linearity
2025/8/1	**Rev 2.0**	Update according to LDMOS die

Application data based on ZBB-23-10/ZXY-23-05/ZBB-23-10

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