

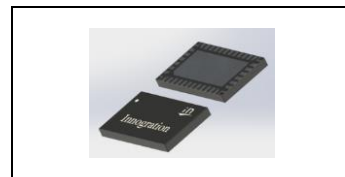


0.1-3.3GHz, 2 stages, 12W, 28V GaN Fully matched PA Module

Description

The G2MAH0133-12 is a 12-watt ,2 stage integrated Power Amplifier Module, designed for broad band applications, with frequencies from 100MHz to 3.3GHz. The module is 50 Ω input/output matched and requires minimal external components.

The module implements distributed power amplifier in form of multi chips, housed in cost effective plastic open cavity package, offers a much lower cost than traditional MMIC solutions.



- Vds=28V, Idq1=10 mA, Idq2=40 mA, CW

Parameter	0.1GHz	0.5GHz	1.0GHz	1.5GHz	2.0GHz	2.5GHz	3.0GHz	3.3GHz	Units
Linear Gain	29.0	26.2	25.7	25.6	25.0	24.1	24.8	24.6	dB
Gain@Pin=19dBm	23.5	23.8	23.5	22.8	22.7	22.3	22.2	21.5	dB
Pout@Pin=19dBm	18.4	18.9	17.7	15.3	14.9	13.4	13.1	12.2	W
PAE@Pin=19dBm	64	61	55	49	48	41	45	45	%

- Vds=32V, Idq1=10 mA, Idq2=40 mA, CW

Parameter	0.1GHz	0.5GHz	1.0GHz	1.5GHz	2.0GHz	2.5GHz	3.0GHz	3.3GHz	Units
Linear Gain	29.5	26.5	26.1	26.0	25.3	24.3	25.3	25.1	dB
Gain@Pin=19dBm	24.4	24.6	24.3	23.6	23.4	22.9	22.9	22.7	dB
Pout@Pin=19dBm	22.7	23.1	21.2	18.4	17.5	15.5	15.4	14.6	W
Eff@Pin=19dBm	64	60	54	48	45	39	44	45	%

Product Features

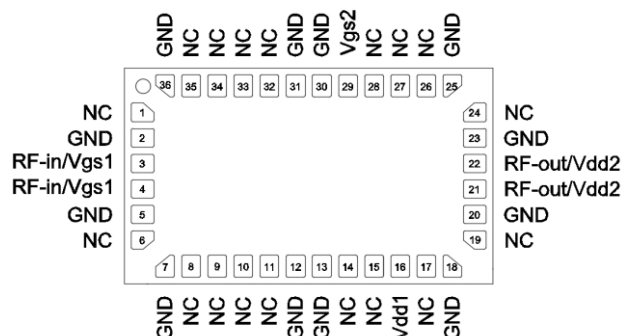
- Operating Frequency Range: 0.1-3.3GHz
- Operating Drain Voltage: +28 V (Up to 32V)
- 50 Ω Input/Output
- Psat: $\geq 12W$ @28V, $\geq 14W$ @32V
- Small signal gain:>24dB, Power gain:>21dB @Pin=19dBm
- Minimum efficiency:>40%
- 6x10 mm Surface Mount Package
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Applications

- Ultra Broadband Amplifiers
- Fiber Drivers
- Test Instrumentation
- EMC Amplifier Drivers
- 2-way Radios



Pin Configuration and Description



Pin No.	Symbol	Description
21,22	RFout/Vdd2	Transistor 1, Drain Bias2 & RF Output
3,4	RFin/Vgs1	Transistor 1, Gate Bias1 & RF Input
29	Vgs2	Transistor 1, Gate Bias2
16	Vdd1	Transistor 1, Drain Bias1
Others	NC	No connection
2,5,7,12, 13,18,20,23,25, 30, 31,36 Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	150	Vdc
Gate--Source Voltage	V_{GS}	-10 to +2	Vdc
Operating Voltage	V_{DD}	+36	Vdc
Input CW Power	RFin	22	dBm
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case, FEA $T_c = 25^\circ\text{C}$, DC test	$R_{\theta JC}$	4.7	°C/W

Table 3. Electrical Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range		100		3300	MHz
Power Gain		21			dB
P_{OUT}	Pin=19dBm		41		dBm
Drain Efficiency @ P_{SAT}		40			%

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_{DD} = 28\text{ V}$, Pulse Width=100 us, Duty cycle=10%Load Mismatch of per Section (On Test Fixture, 50 ohm system): $V_{DD} = 28\text{ V}$, $I_{DQ} = 90\text{ mA}$, $f = 3\text{ GHz}$

VSWR 10:1 at pulse CW Output Power @Pin=22dBm	No Device Degradation
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Reference Circuit of Test Fixture Assembly Diagram

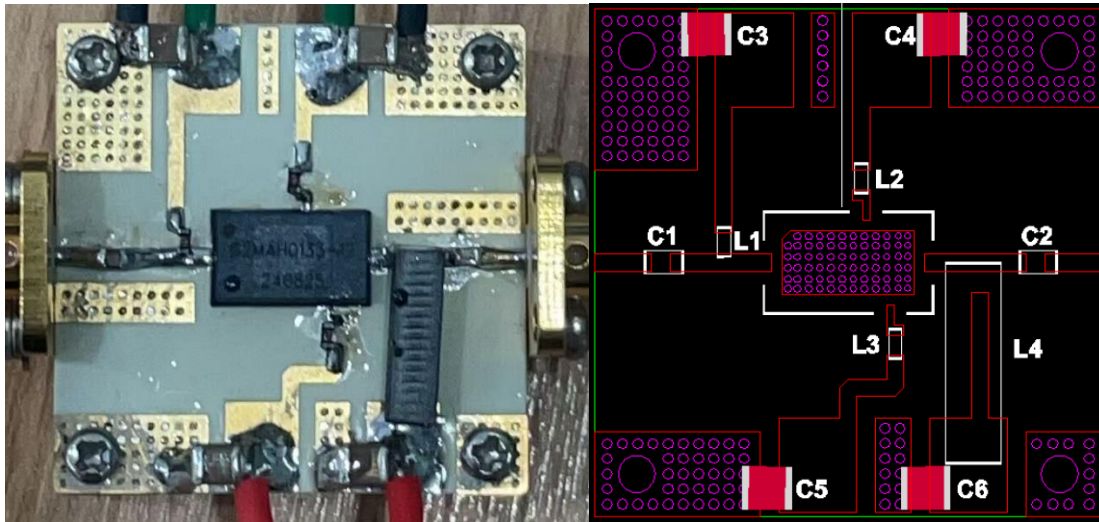


Figure 1. Test Circuit Component Layout

		Part NO.	Vendor
C1, C2	50V 1uF Chip Capacitor	GRM21BR71H105KA12L	muRata
C3,C4,C5,C6	10uF 100V Chip Capacitor	C5750X7S2A106M230KB	TDK
L1, L2,L3	100 nH Capacitor(0603)	LQW18CNR10K00D	muRata
L4	1.3uH 4.2A Inductor	4310LC-132KEC	Coilcraft
PCB	RO4350B,20mil,er=3.48		

TYPICAL CHARACTERISTICS

Figure 2. Network analyzer output S11/S21 (VDS= 28V, IDQ1=10 mA, IDQ2=40 mA Pin=0dBm)

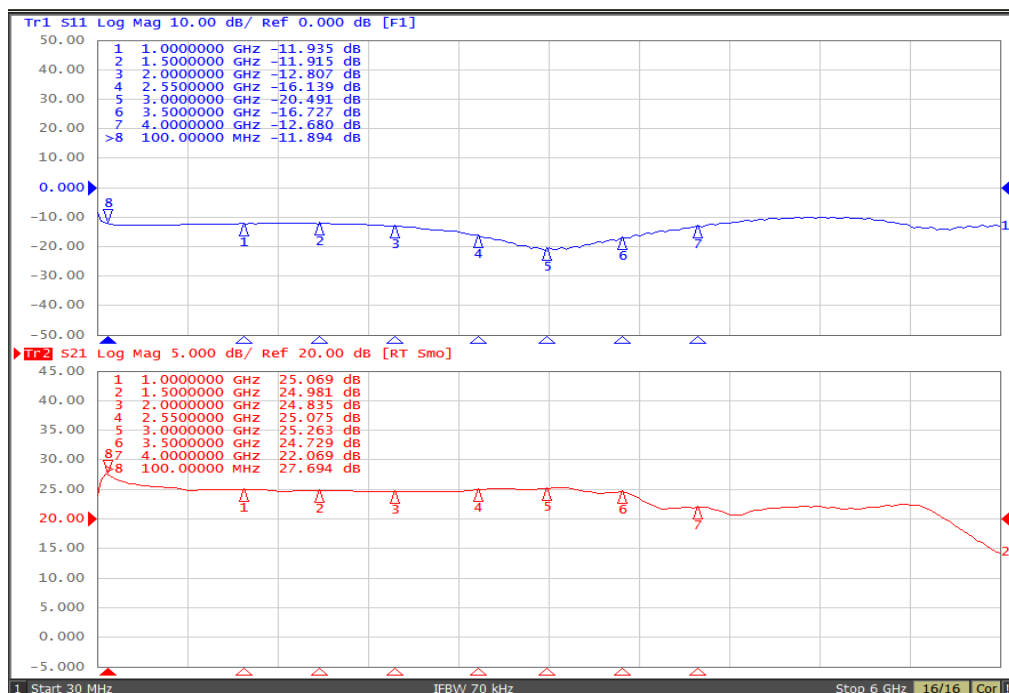




Figure 3. Power Gain and, efficiency and Pout @Pin=19dBm, P3dB vs. Frequency

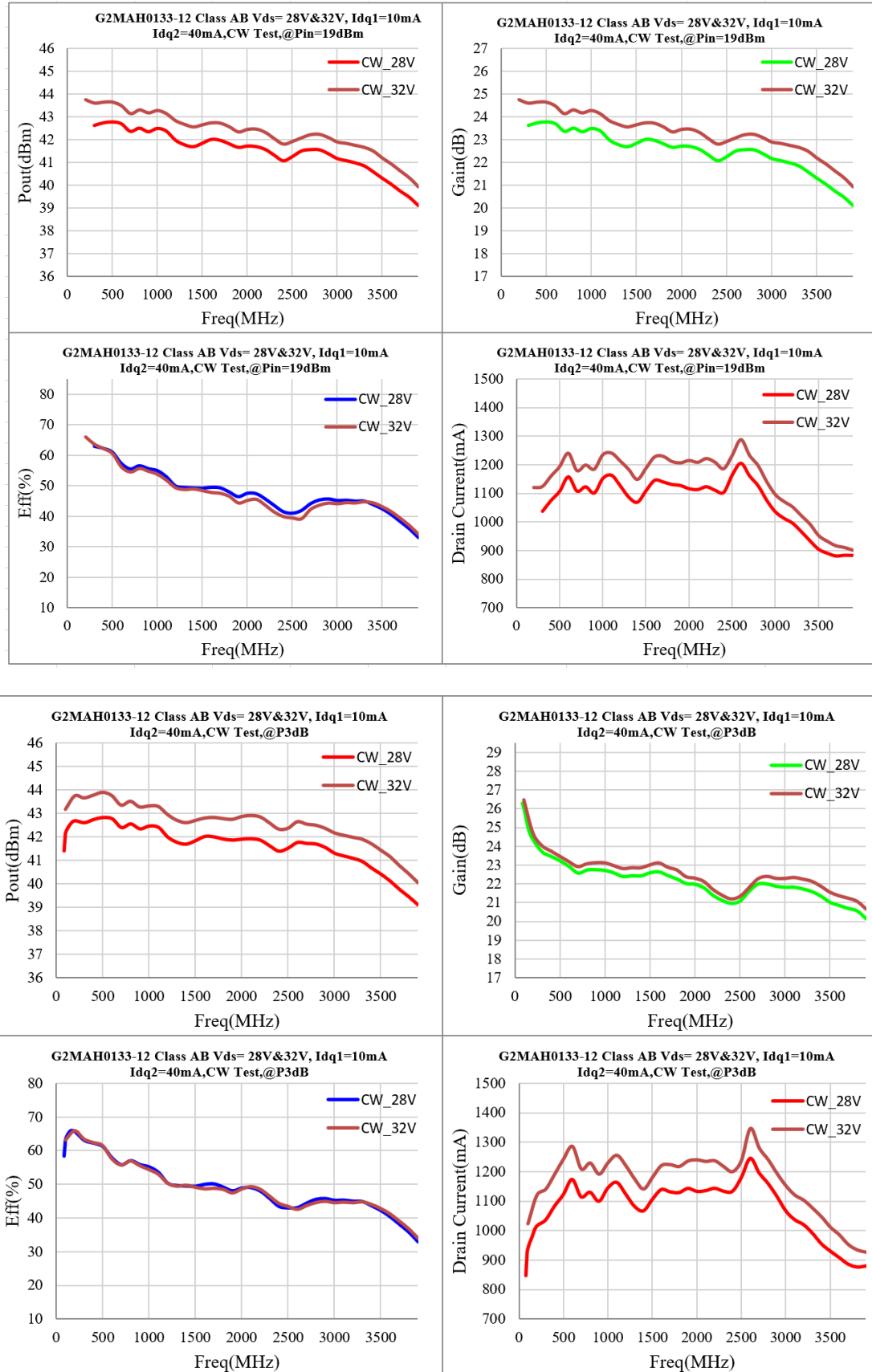
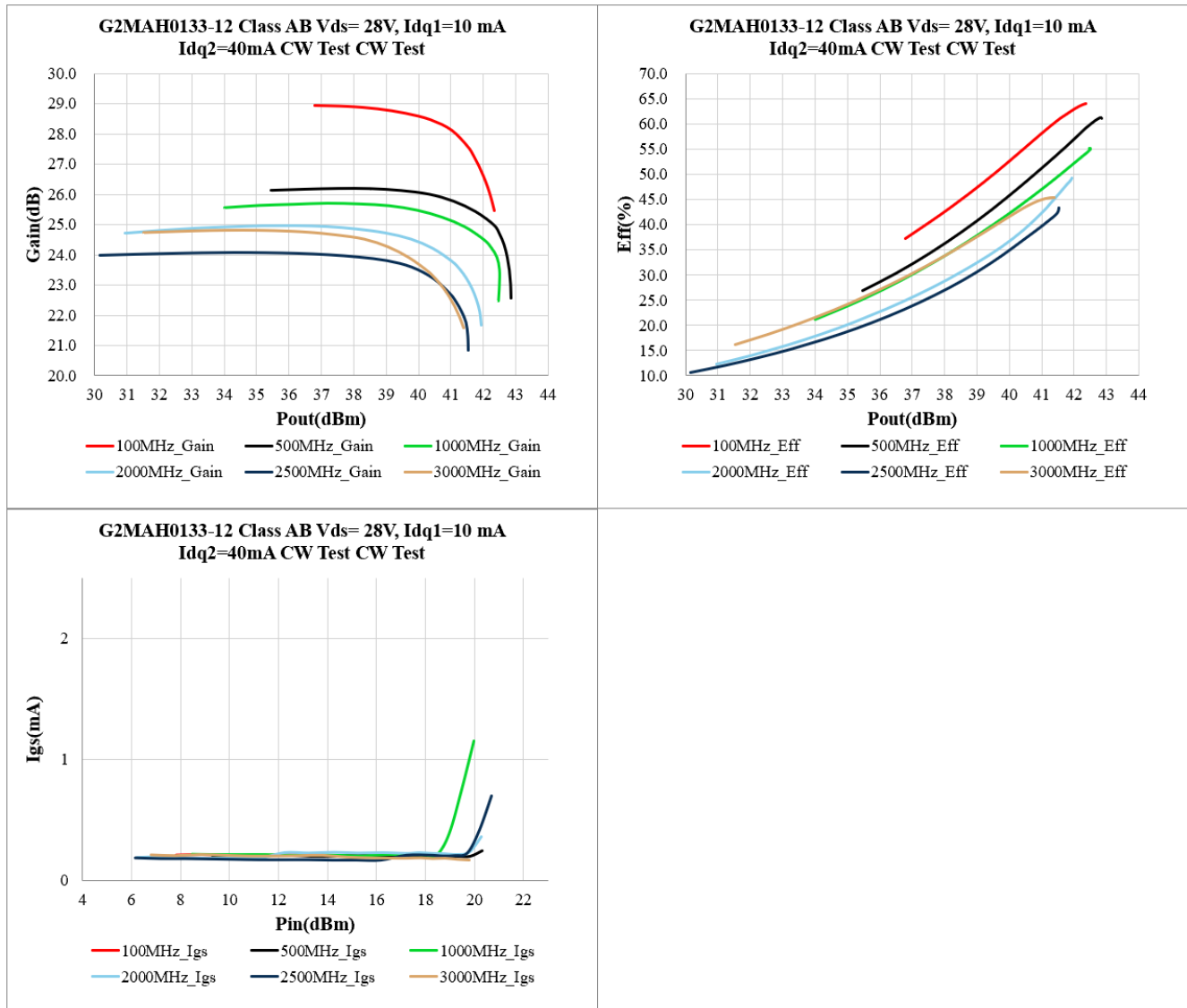




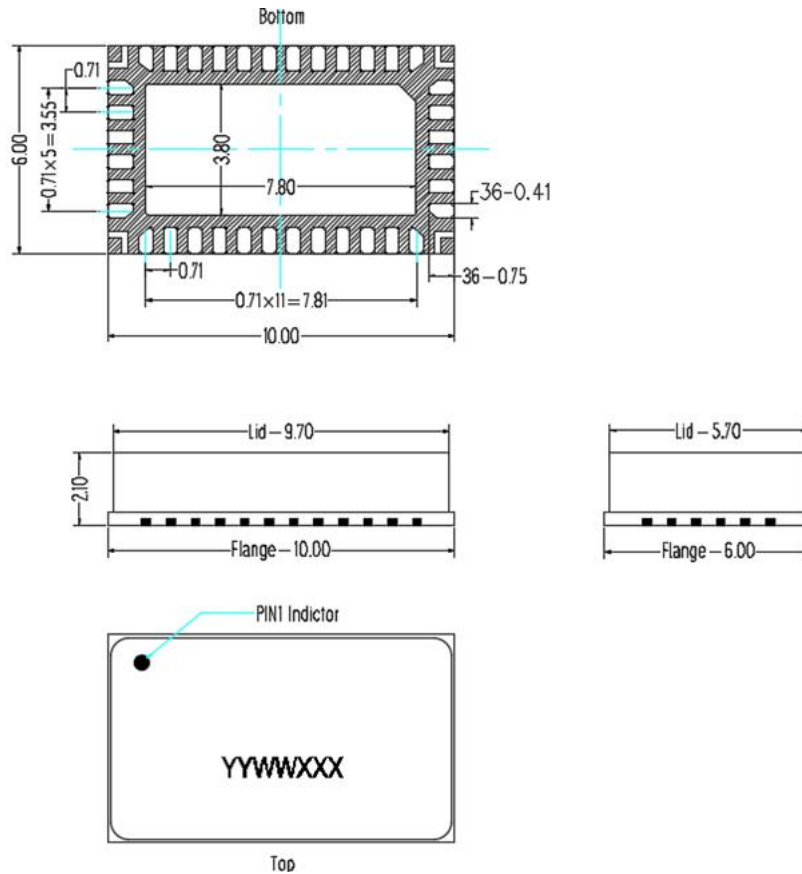
Figure 4. AM/AM Plot





Package Dimensions

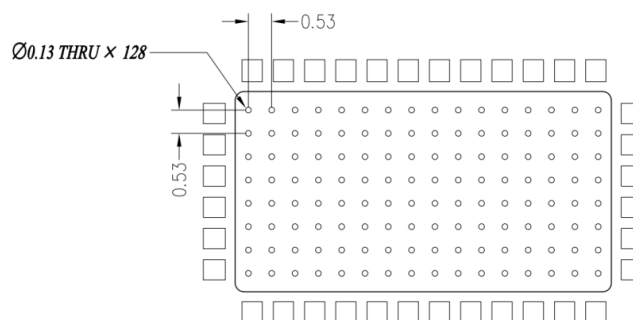
10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ± 0.2 mm.

Mounting Footprint Pattern



Notes:

1. All dimensions are in mm;
2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. ALL vias are PTH to ground.



Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2023/7/6	Rev 1.0	Preliminary Datasheet Creation
2025/5/16	Rev 2.0	Modify the PCB layout by split of Vgs1 and Vgs2

Application data based on ZHH-23-12/25-04

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