S3C111K2VS GaN TRANSISTOR

Document Number: S3C111K2VS
Preliminary Datasheet V1.0

1030-1090MHz, 1200W, GaN RF Power Transistor

S3C111K2VS

Description

The S3C111K2VS is a 1200-watt, high performance, internally matched GaN RF Power transistor, designed for multiple applications with frequencies from 1030-1090MHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as Avionics application, within L band

Supported by high breakdown voltage, it is also usable at higher voltage up to 55V, with higher output power.

•Typical **Pulsed CW** Performance (On Innogration fixture with device soldered):

V_{DD} = 50 Volts, I_{DQ} = 150mA, Pulse CW, Pulse width=20us, Duty cycle=10%.

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1060	60.74	1185.9	71.8	20.68	61.12	1295.1	73.6

Applications and Features

- Suitable for L band pulse amplifier, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage (50V)
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to 0	Vdc
Operating Voltage	V_{DD}	0 to 55	Vdc
Maximum forward gate current	Igf	141	mA
Storage Temperature Range	Tstg	-65 to +150	C
Case Operating Temperature	T_C	-55 to +150	C
Operating Junction Temperature	T_J	+225	C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case 85 °C Case backside Temperature Pout = 1200 W, Pulse: 20 us PW, 10% DC	$R_{\theta JC}$	0.2	C/W

Table 3. Electrical Characteristics (T_C = 25℃ unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS}=-8V; I_{DS}=141mA	V_{DSS}		200		V
Gate Threshold Voltage	V_{DS} = 50V, I_D = 141mA	V_{GS}(th)	-4		-2	V
Gate Quiescent Voltage	V_{DS} =50V, I_{DS}=150mA, Measured in Functional Test	$V_{GS(Q)}$		-3.3		V

Functional Tests (In Innogration broadband Test Fixture, 50 ohm system) : V_{DD} = 50 Vdc, I_{DQ} = 150 mA, f = 1060 MHz, Pulse CW

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @ P3dB	Gp		17		dB
Drain Efficiency@P3dB$_t$	Eff		70		%
3dB Compressed point	P3dB		1200		W
Input Return Loss	IRL		-7		dB
Mismatch stress at all phases(No device damage)	VSWR		10:1		Ψ

Reference Circuit of Test Fixture Assembly Diagram

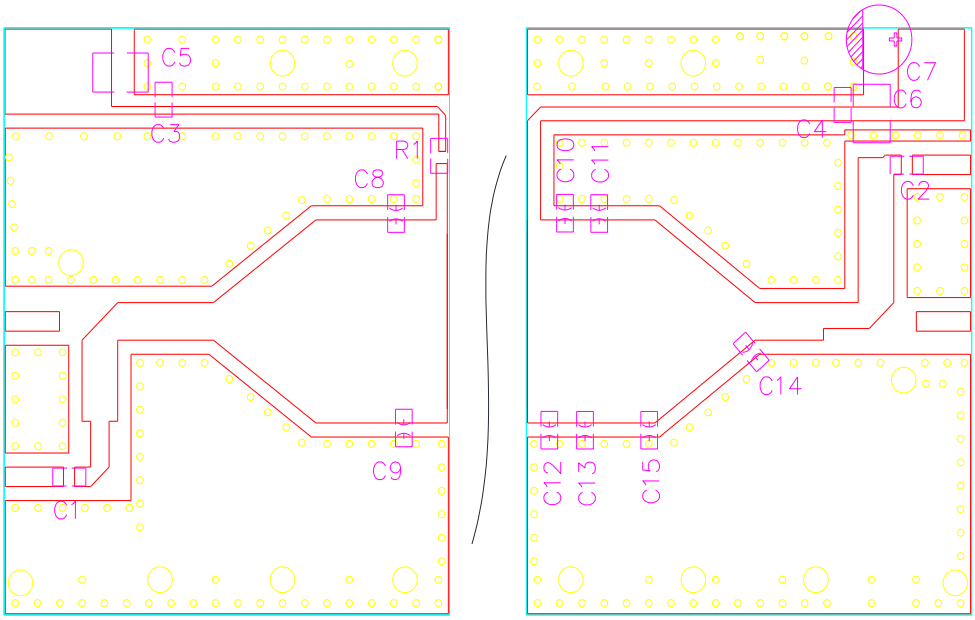


Figure 1. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Designator	Comment	Footprint	Quantity
C1	2.7pF/250V	0603/0805	1
C2, C3, C4	43 pF/250V	0805	3
C5, C6	10uF/100V	1210	2
C7	100uF/63V		1
C8, C9, C10, C11, C12	8.2pF/250V	0603/0805	5
C13, C14	6.8pF/250V	0603/0805	2
C15	2.2pF/250V	0603/0805	1
R1	10 Ω	0603	1

TYPICAL CHARACTERISTICS

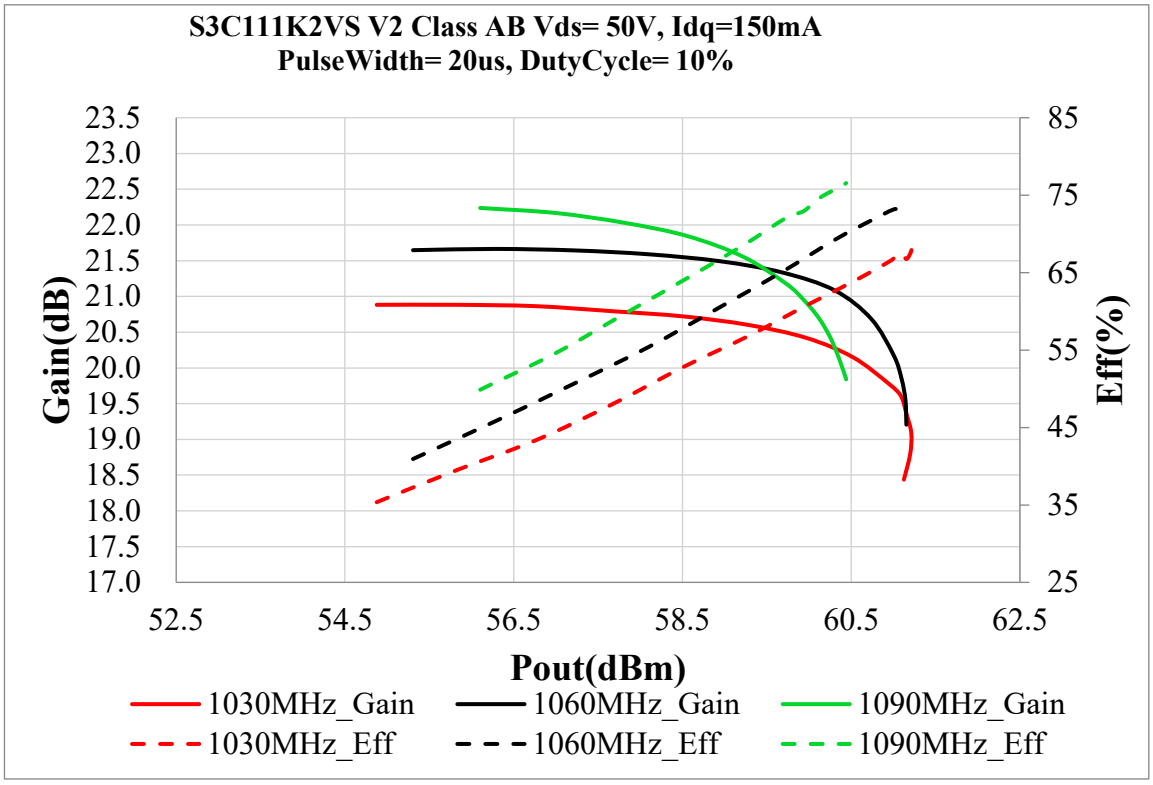


Figure 2. Power Gain and Drain Efficiency as Function of Pulse Output Power（1030-1090MHz）

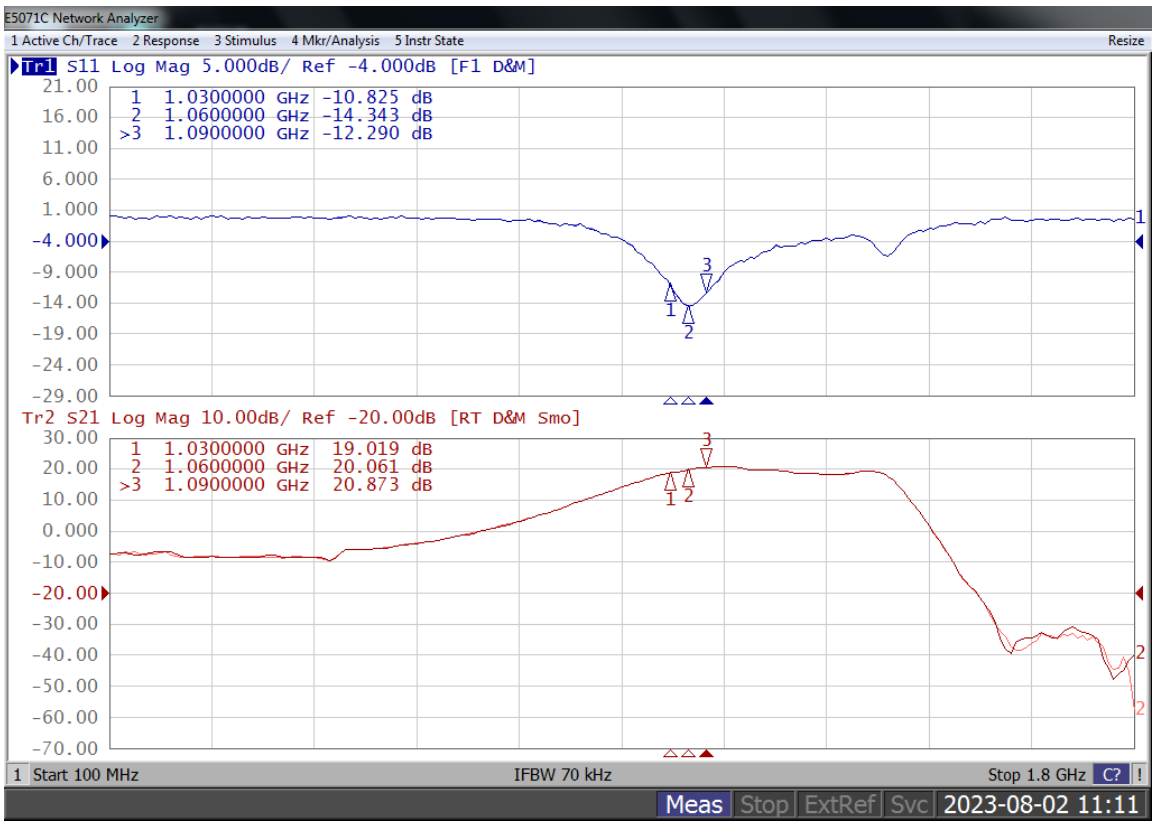
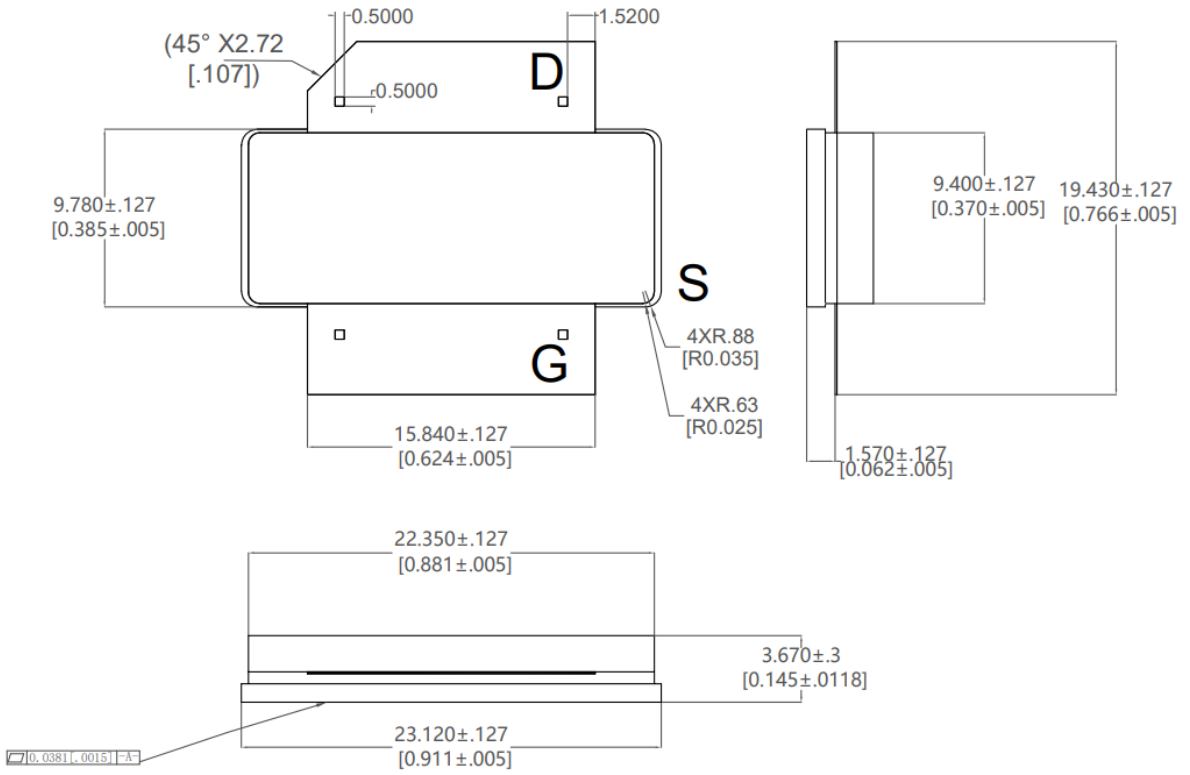


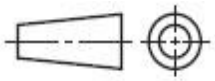
Figure 3. Network analyzer output S11/S21

Package Outline

Flangeless ceramic package;

INP-688-2-EL（C2)



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2023/8/2	Rev 1.0	Preliminary Datasheet

Application data based on LSM-23-25

Disclaimers