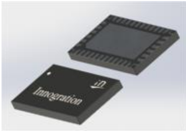
# Gallium Nitride 50V, 55W, 3.4-4GHz RF Power Transistor

**STAV40055C6**



## Description

The STAV40055C6 is a 55-watt, internally matched GaN HEMT, designed for 5G cellular applications with frequencies from 3.4-4GHz.It can be configured as asymmetrical Doherty for 4G or 5G application, delivering 8 to 9W average power, according to normal 8 to 9dB back off. There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.

- Typical Doherty Pulsed CW and 1C W--CDMA Characterization Performance:

$V_{DD}$ = 50 Vdc, $I_{DQA}$ = 50 mA, $V_{GSB}$ = –5.1Vdc,

(1)Pulsed condition: 20us and 10%,

(2)1C WCDMA; Signal PAR = 10 dB @ 0.01% Probability on CCDF.

| Freq (GHz) | Pulse CW Signal(1) | | | $P_{avg}$=39dBm WCDMA Signal(2) | | |
|---|---|---|---|---|---|---|
| | P1-Gain (dB) | P3 (dBm) | P3 (W) | Gp (dB) | $\eta_D$ (%) | $ACPR_{5M}$ (dBc) |
| 3.4 | 12.92 | 48.36 | 68.6 | 13.03 | 49.85 | -28.03 |
| 3.5 | 13.47 | 48.33 | 68.3 | 13.55 | 47.00 | -30.87 |
| 3.6 | 13.78 | 48.07 | 64.2 | 14.08 | 46.35 | -32.89 |
| 3.7 | 14.55 | 47.86 | 60.5 | 14.69 | 47.15 | -32.79 |
| 3.8 | 15.45 | 47.80 | 60.2 | 15.19 | 48.55 | -31.97 |
| 3.9 | 14.87 | 47.65 | 58.2 | 14.43 | 48.50 | -31.27 |
| 4.0 | 13.47 | 47.75 | 60.0 | 13.19 | 47.23 | -32.64 |

## Applications

- 5G, 4G wireless infrastructure
- Wideband or narrowband power amplifier
- Test instruments
- S band power amplifier

## Important Note: Proper Biasing Sequence for GaN HEMT Transistors

**Turning the device ON**

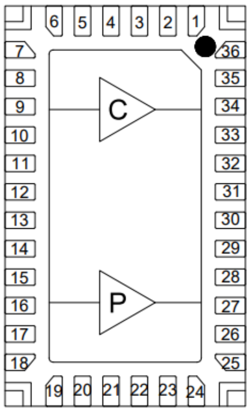
1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

**Turning the device OFF**

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

**Figure 1: Pin Connection definition**

**Transparent top view (Backside grounding for source)**




| Pin No. | Symbol | Description |
|---|---|---|
| 8,9 | RF IN/Vgs1 | RF Input, Vgs bias for carrier path |
| 15,16,17 | RF IN/Vgs2 | RF Input, Vgs bias for peak path |
| 1 | VDD1 | VDD bias for Carrier path |
| 24 | VDD2 | VDD bias for Peak path |
| 34,35 | RF Out 1 | RF Output for main path |
| 27,28 | RF Out 2 | RF Output for Peak path |
| Rest pins | NC | No connection |
| 2,5,7,12,13,18,20,23,25,30,31,36, Package Base | GND | DC/RF Ground. Must be soldered directly to heatsink or copper coin for CW application. |

**Table 1. Maximum Ratings**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain--Source Voltage | $V_{DSS}$ | +200 | Vdc |
| Gate--Source Voltage | $V_{GS}$ | -8 to +0.5 | Vdc |
| Operating Voltage | $V_{DD}$ | 55 | Vdc |
| Maximum gate current | Igs | 9 | mA |
| Storage Temperature Range | Tstg | -65 to +150 | °C |
| Case Operating Temperature | $T_C$ | +150 | °C |
| Operating Junction Temperature | $T_J$ | +225 | °C |

**Table 2. Thermal Characteristics**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Case by FEA $T_C$= 85°C, Pdiss=9W at Pavg=39dBm WCDMA 1 carrier | RθJC | 6 | °C /W |

Notes: Based on expected carrier amplifier efficiency of Doherty, Pavg assumes 10% peaking amplifier contribution of total average Doherty rated power. Thermal resistance is measured to package backside

**Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)**

**DC Characteristics (main path, measured on wafer prior to packaging)**

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | VGS=-8V; IDS=3mA | $V_{DSS}$ | | 200 | | V |
| Gate Threshold Voltage | VDS =10V, ID = 3mA | $V_{GS(th)}$ | -4 | | -2 | V |
| Gate Quiescent Voltage | VDS =50V, IDS=45mA, Measured in Functional Test | $V_{GS(Q)}$ | | -3.1 | | V |

**DC Characteristics (peak path, measured on wafer prior to packaging)**

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | VGS=-8V; IDS=5mA | $V_{DSS}$ | | 200 | | V |
| Gate Threshold Voltage | VDS =10V, ID = 5mA | $V_{GS(th)}$ | -4 | | -2 | V |
| Gate Quiescent Voltage | VDS =50V, IDS=60mA, Measured in Functional Test | $V_{GS(Q)}$ | | -3.1 | | V |

**Ruggedness Characteristics**

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Load mismatch capability | 3.8GHz, Pout=39dBm WCDMA 1 Carrier, All phase, No device damages | VSWR | | 10:1 | | |

**Figure 2: Efficiency and power gain as function of Pout (**Measured on 3.4-4GHz Doherty board)

$V_{DD}$ = 50 Vdc, $I_{DQ}$ = 50mA, Pulse width=50us, duty cycle=20%

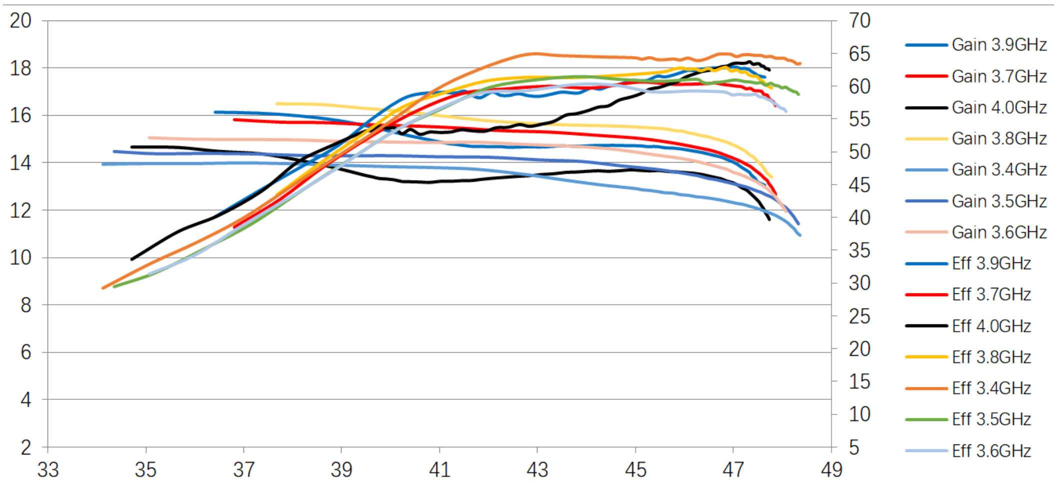



**Figure 3: Network plot for S11/S21**

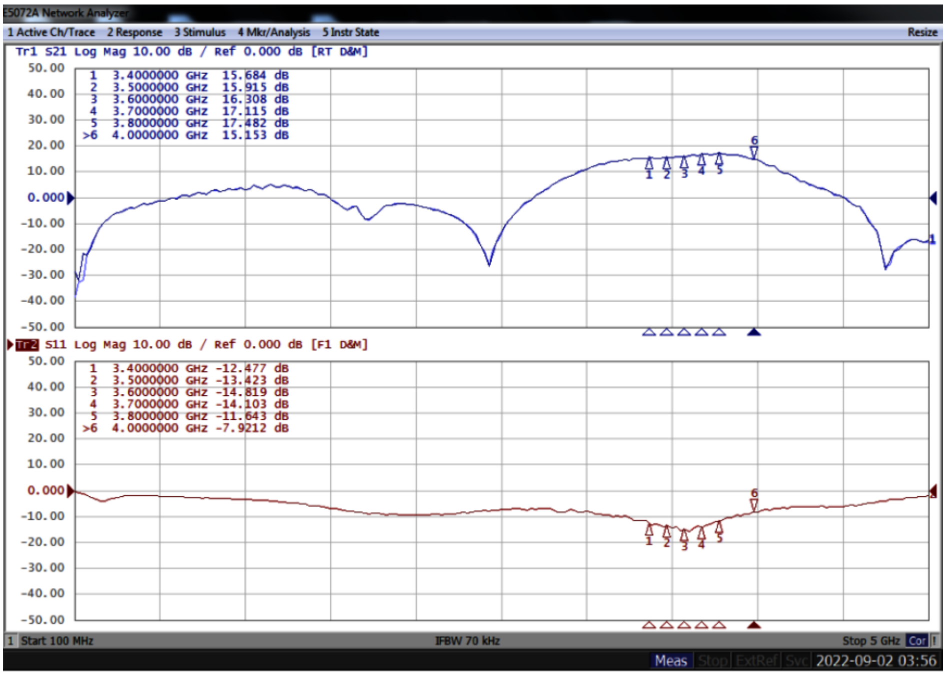


**Figure 4: Picture of application board of 3.4-4GHz Doherty**

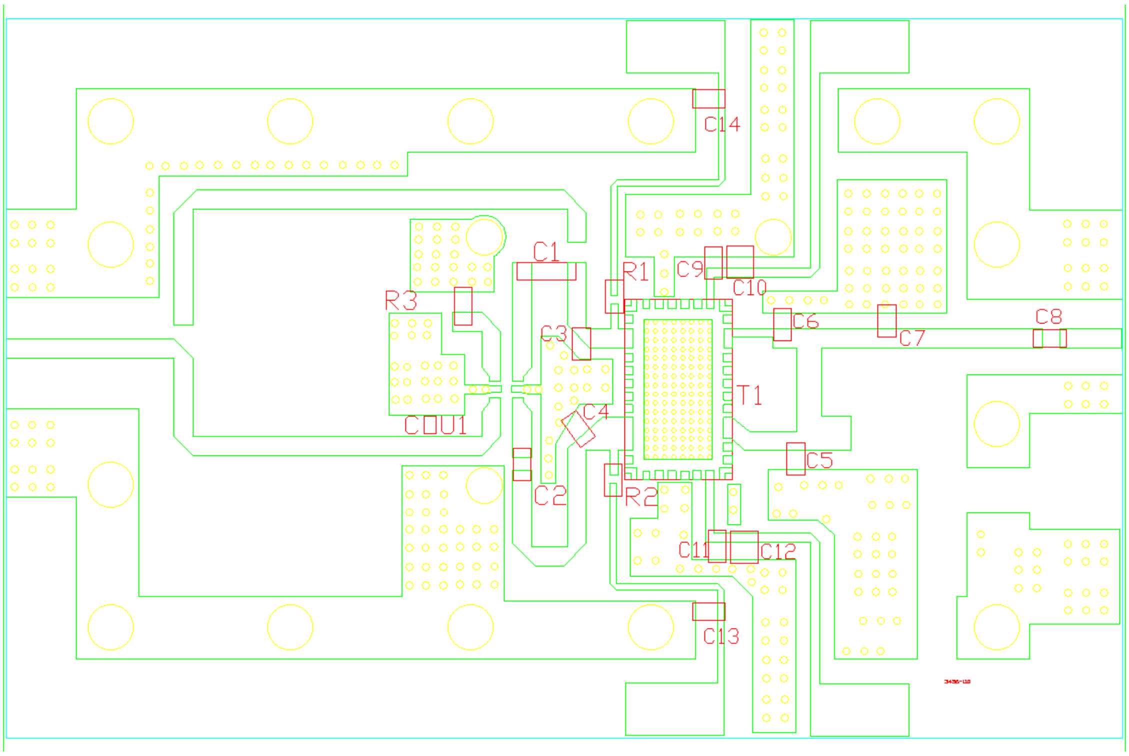
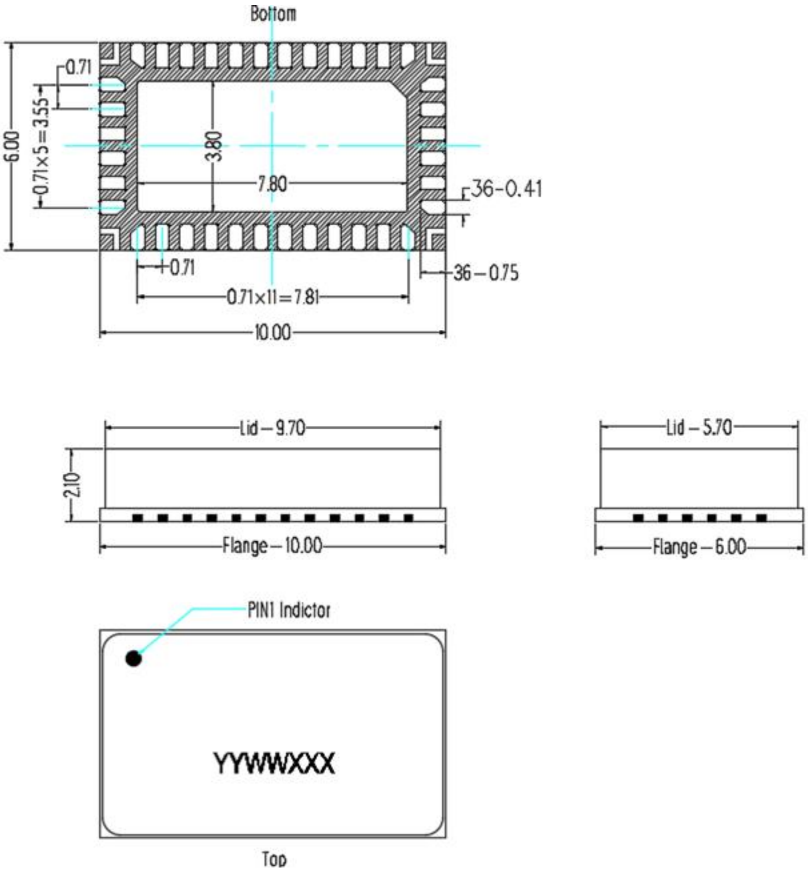



**Table 4. Bill of materials of application board (RO4350B 20mils, PCB layout upon request)**

| Part | Quantity | Description | Part Number | Manufacture |
|---|---|---|---|---|
| C1,C2,C8, C9,C11,C13,C14 | 7 | 8.2pFHigh Q Capacitor | 251SHS8R2BSE | TEMEX |
| C3,C4 | 2 | 1.2pFHigh Q Capacitor | 251SHS1R2BSE | TEMEX |
| C5 | 1 | 0.7pFHigh Q Capacitor | 251SHS0R7BSE | TEMEX |
| C10,C12 | 2 | 10uF MLCC | GRM32EC72A106ME05 | Murata |
| C6,C7 | 2 | 0.6pFHigh Q Capacitor | 251SHS0R6BSE | TEMEX |
| R1,R2 | 1 | 10Ω Power Resistor | ESR03EZP10R0 | ROHM |
| R3 | 1 | 51Ω Power Resistor | S1206N | RN2 |
| COUT1 | 1 | 3 dB Bridge | C3337J5003AF | ANAREN |
| T1 | 1 | 55W GaN Dual Transistor | STAV40055C6 | Innogration |

## Package Dimensions

### 10*6 Plastic Package




Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.2mm.

## Revision history

**Table 4. Document revision history**

| Date | Revision | Datasheet Status |
|---|---|---|
| **2022/9/6** | **V1.0** | **Preliminary Datasheet Creation** |
| **2022/12/9** | **V1.1** | **Update on Pin Definition** |

**Application data based on: LWH-22-17**

## Notice

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