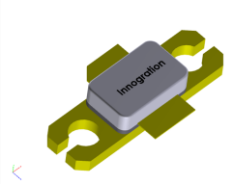
S3U1045V GaN TRANSISTOR

Document Number: S3U1045V
Preliminary Datasheet V1.1

Gallium Nitride 50V 450W, RF Power Transistor

S3U1045V



Description

The S3U1045V is a 450W single ended GaN HEMT, designed for multiple applications with frequencies up to 1.0GHz. **It offers much smaller and simpler matching circuit than traditional push-pull matching circuit ,as key benefit to customers.**

It is recommended to use this part for pulsed CW application only.

There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.

•Typical performance (on Innogration narrow band production fixture with device soldered)

S3U1045V, Vds=50V, Idq=130mA ,Vgs=-3.22V 100us/10%						
F(MHz)	Pin（dBm）	Psat（dBm）	Psat（W）	I(A)	Gain（dB）	Eff(%)
425	34	57.31	538.27	1.53	23.3	70.4
435	34	57.22	527.23	1.49	23.2	70.8
445	33.7	57.16	520.00	1.42	23.5	73.2
455	32.2	57.00	501.19	1.34	24.8	74.8
465	32.6	56.52	448.75	1.22	23.9	73.6
475	32.7	56.16	413.05	1.11	23.5	74.4

Applications and Features

- Suitable for wireless communication infrastructure, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage (50V)
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+150	Vdc
Gate--Source Voltage	V_{GS}	-8 to 0	Vdc
Operating Voltage	V_{DD}	0 to 55	Vdc
Maximum forward gate current	Igf	54	mA
Storage Temperature Range	Tstg	-65 to +150	C
Case Operating Temperature	T_C	-55 to +150	C
Operating Junction Temperature	T_J	+225	C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit

Thermal Resistance, Junction to Case T_C= 85°C, DC Power Dissipation, FEA	$R_{\theta JC}$	0.7	C/W

Table 3. Electrical Characteristics (T_C = 25℃ unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS}=-8V; I_{DS}=54mA	V_{DSS}		150		V
Gate Threshold Voltage	V_{DS} = 50V, I_D = 54mA	V_{GS}(th)		-3.4		V
Gate Quiescent Voltage	V_{DS} =50V, I_{DS}=100mA, Measured in Functional Test	$V_{GS(Q)}$		-3.2		V

Reference Circuit of Test Fixture Assembly Diagram

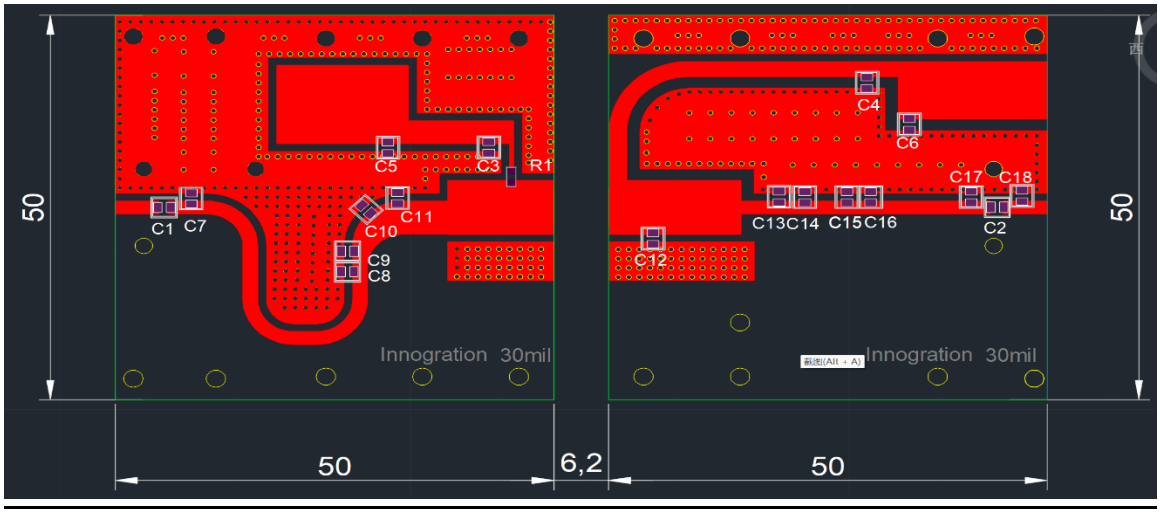
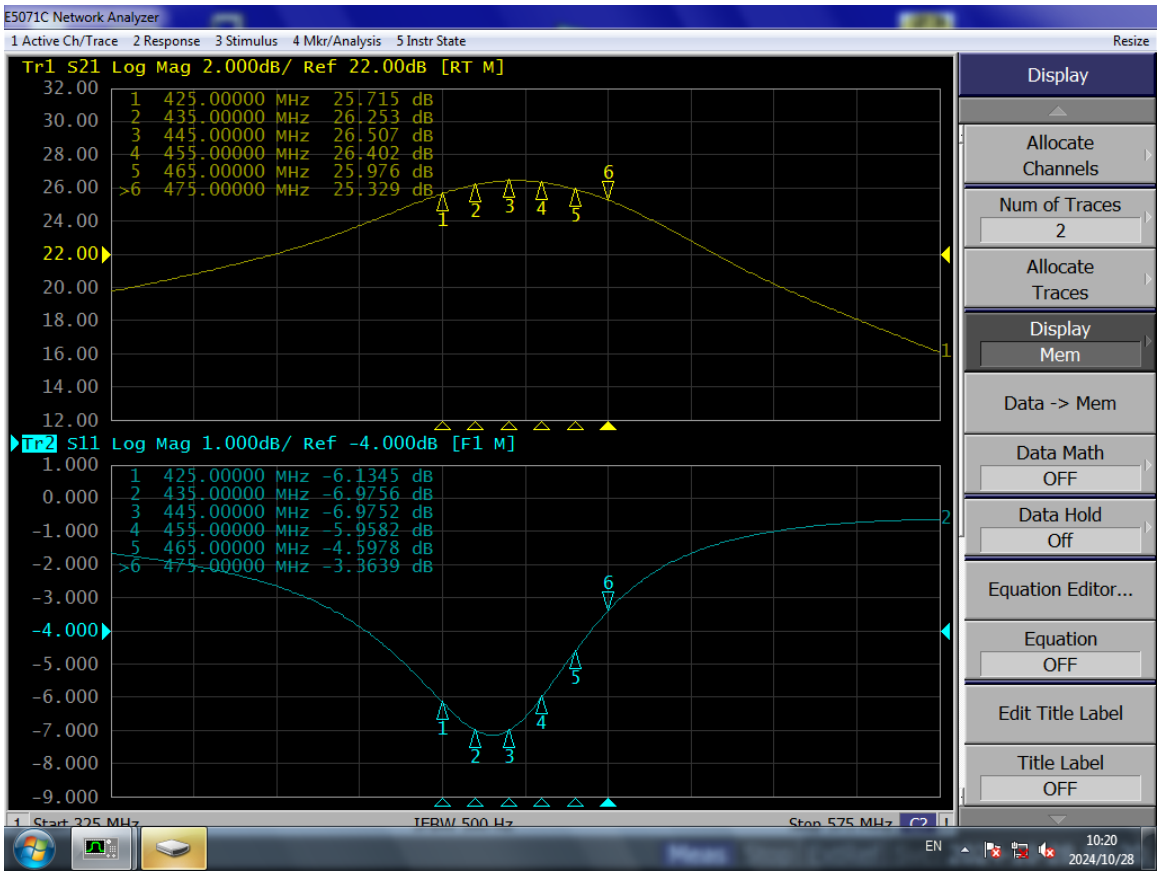


Figure 1. Test Circuit Component Layout (425-475MHz) RO4350B 30mils

Table 4. Test Circuit Component Designations and Values

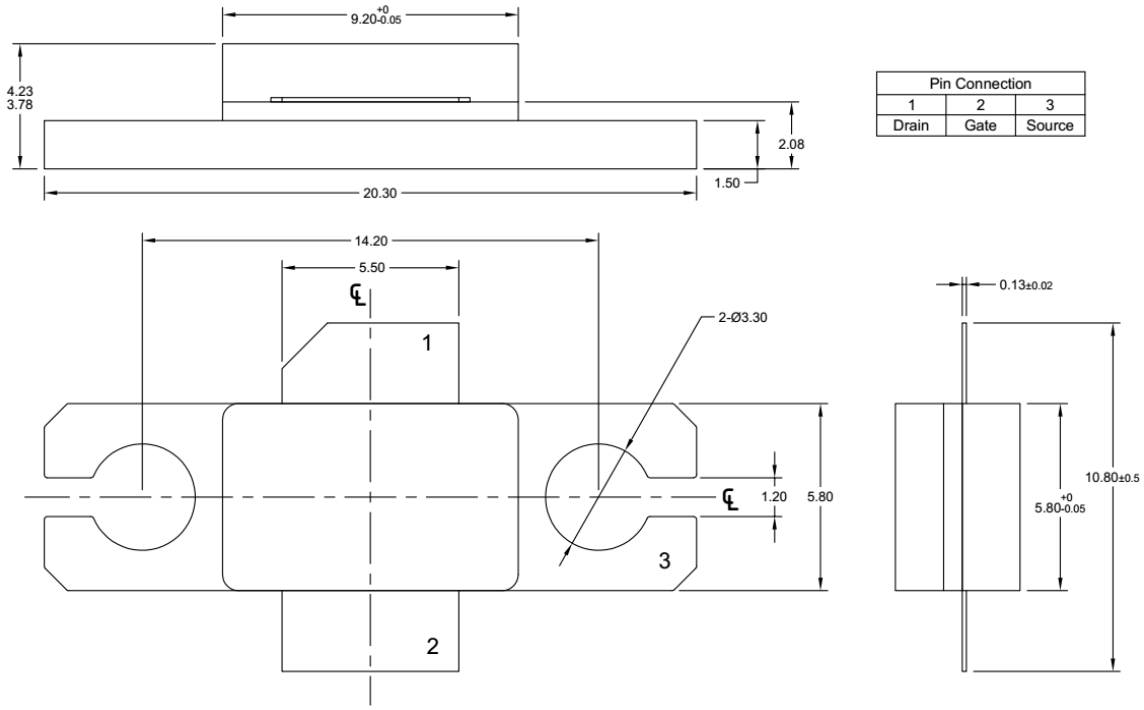
Component	Description	Suggestion
C5,C6	10uF 1210	/
R1	51Ω 0805	/
C1,C2	82pF MQ301111	BJYL
C3,C4	1000pF MQ301111	BJY
C7	1.8pF MQ301111	BJYL
C8,C9,C14	10pF MQ301111	BJYL
C10	22pF MQ301111	BJYL
C11,C13	15pF MQ301111	BJYL
C12	2.2pF MQ301111	BJYL
C15	3.6pF MQ301111	BJYL
C16,C18	3.0pF MQ301111	BJYL
C17	4.3pF MQ301111	BJYL
L1	01mm wire ， 5mm inner diameter, 5Turns	DIY

Figure 2. Network Analyzer result S11 and S21 Vgs = -3.1V, VDS= 50V, IDQ = 400mA



Package Outline

Flanged ceramic package; 2 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-GXB					10/10/2017

Figure 1. Package Outline PKG-G2E

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/9/7	V1.0	Preliminary Datasheet
2024/10/28	V1.1	Change application to 425-475MHz

Application data based on SYX-23-43/24-38

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