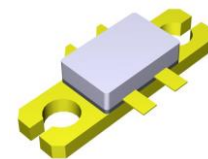




80-1000MHz, 20W, 50V LDMOS matched PA Module

Description

The IMGV0110-25G4E is a 20-watt, single stage, Power Amplifier designed for broad band applications, with frequencies from 80MHz to 1GHz. The module is 50 Ω input matched and requires minimal external components at output.



V_{ds}=50V, I_{dq}=150mA, CW

Freq (MHz)	P _{out} (W)	I _{ds} (A)	P _{in} (dBm)	Gain (dB)	Eff (%)	2 nd (dBc)	3 rd (dBc)
80	29.9	0.91	36	8.76	65.76	-11.5	-12.7
100	30.5	0.85	35.95	8.9	71.88	-13.6	-12.7
200	30.3	0.84	35.97	8.85	72.24	-21.5	-14
300	28.7	0.99	35.53	9.05	58.00	-17.5	-15.3
400	27.0	1.13	36.09	8.22	47.75	-15.3	-17.8
500	24.8	1.19	36.89	7.06	41.73	-15.7	-21.2
600	26.1	1.21	37.04	7.13	43.18	-18.3	-22.1
700	28.4	1.16	36.6	7.94	49.04	-22.8	-25.4
800	29.1	1.09	35.21	9.43	53.41	-29	-29.5
900	27.3	1.08	36.37	7.99	50.54	-35.9	-30.8
1000	21.9	1.10	36.43	7.01	40.01	-25.5	-34

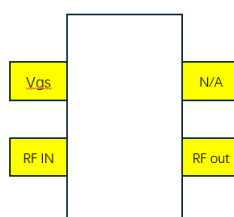
Product Features

- Operating Frequency Range: 80M-1GHz
- Operating Drain Voltage: +50 V
- 50 Ω Input
- P_{sat}: ≥ 20 W(CW)
- Small signal gain:>11dB, Power gain:>7dB @50V
- Minimum efficiency:>35% @50V
- Much lower cost than GaN-based ultrawide band PA, due to LDMOS technology used

Applications

- Ultra Broadband Amplifiers
- Driver for ISM, FM
- Test Instrumentation
- HF/VHF 2-way Radios

Pin Configuration and Description



Top View



Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+50	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c = 25^\circ\text{C}$, CW Pout=20W@0.5GHz	$R_{\theta JC}$	1.8	°C/W

Table 3. Electrical Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range	Pin=36.5dBm	80		1000	MHz
Power Gain @ Psat	Pin=36.5dBm	7		9	dB
P_{OUT}	Pin=36.5dBm	43		45	dBm
Drain Efficiency @ P_{SAT}	Pin=36.5dBm	35			%

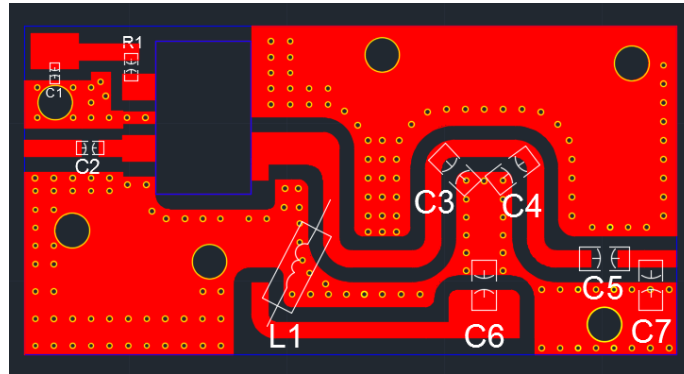
Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_{DD} = 50\text{ V}$, Pulse Width=100 us, Duty cycle=10%

Load Mismatch of per Section (On Test Fixture, 50 ohm system): $V_{DD} = 50\text{ V}$, $I_{DQ} = 150\text{ mA}$, $f = 0.5\text{ GHz}$

VSWR 10:1 at Psat pulse CW Output Power	No Device Degradation
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Reference Circuit of Test Fixture Assembly Diagram



C1,C6	10uF/0805	/
C2,C5	560pF/MQ301111	BEIJING YUANLU HONGYUAN ELECTRONICTECHNOLOGY CO., LTD
C3	0.5pF/MQ40-0805	BEIJING YUANLU HONGYUAN ELECTRONICTECHNOLOGY CO., LTD
C4	2.0pF/MQ40-0805	BEIJING YUANLU HONGYUAN ELECTRONICTECHNOLOGY CO., LTD
C7	1.5pF/MQ40-0805	BEIJING YUANLU HONGYUAN ELECTRONICTECHNOLOGY CO., LTD
R1	220Ω/0805	/
L1	0.8mm φ=4mm-1.5mm 10turns	DIY

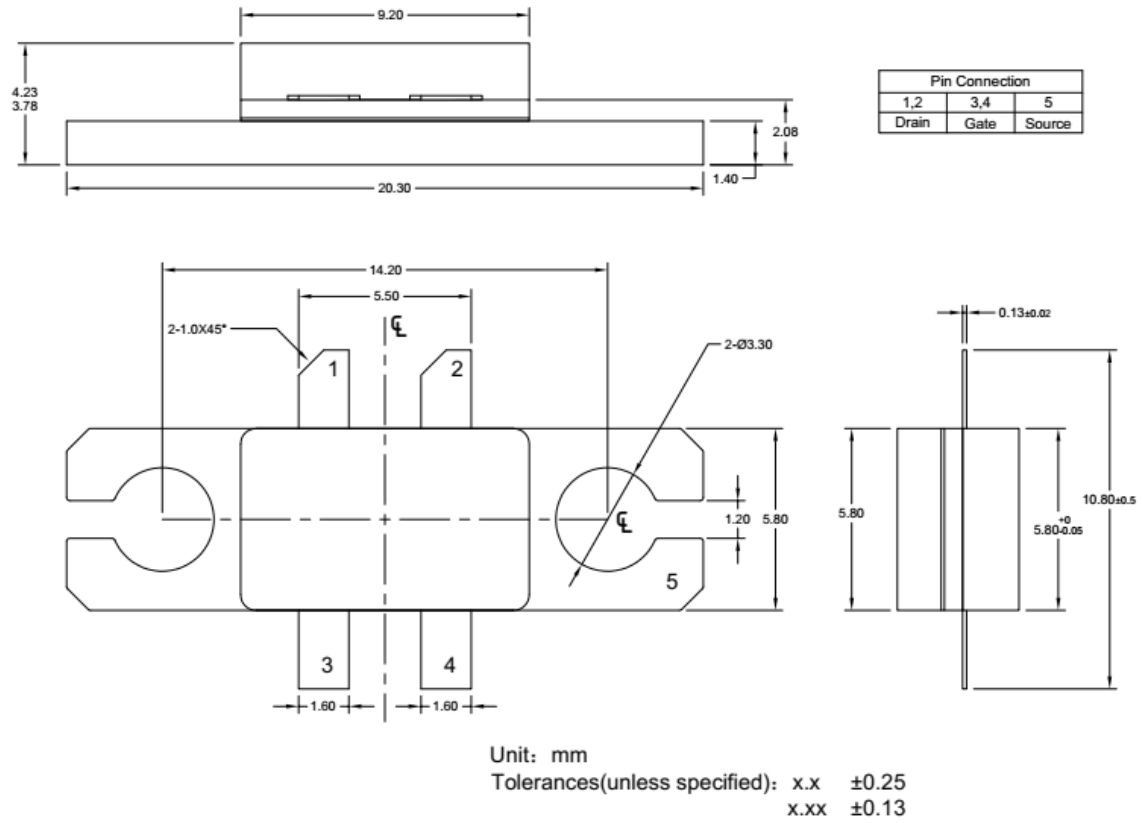
TYPICAL CHARACTERISTICS

Figure 1. Network analyzer output S11/S21 (Pin=0dBm) @50V



Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



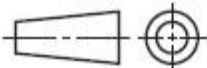
OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-G4E					2018/01/19

Figure 1. Package Outline PKG-G4E



Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2024/12/4	Rev 1.0	Production Datasheet

Application data based on SJJ-24-17

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