



GaN 50V,400W, RF Power Transistor

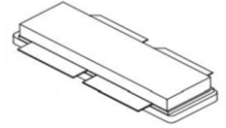
Description

The S3Q3040RVPS is a push pull 480W capable, internally matched GaN HEMT, ideal for multiple applications up to 3GHz. It is optimized thermally to support higher duty cycle or longer pulse up to CW application.

In typical wideband application from 0.2 to 1GHz, it can deliver >400W with high efficiency across the full band.

There is no guarantee of performance when this part is used outside of stated frequencies.

S3Q3040RVPS



- Typical CW performance at 0.2-1GHz applications

S3Q3040RVPS ^{V0} Vgs=-4.0V Vds=50V Idq=10mA CW								
Freq (MHz)	Psat (dBm)	Psat (W)	Ids (A)	Pin (dBm)	Gain (dB)	Eff (%)	2nd (dBc)	3rd (dBc)
200	56.47	443.6	12.90	37.64	18.83	68.78	-35.90	-10.20
250	56.80	478.6	13.47	37.61	19.19	71.07	-39.20	-9.80
300	56.51	447.7	12.60	37.72	18.79	71.07	-35.50	-9.10
350	56.46	442.6	12.79	37.15	19.31	69.21	-31.40	-9.10
400	56.31	427.6	12.82	37.96	18.35	66.70	-40.40	-8.10
450	56.41	437.5	13.47	37.00	19.41	64.96	-32.30	-8.80
500	56.21	417.8	13.46	38.61	17.60	62.08	-39.20	-10.10
550	56.66	463.4	13.74	37.68	18.98	67.46	-36.20	-15.30
600	56.74	472.1	13.70	38.42	18.32	68.91	-31.30	-22.30
650	56.76	474.2	14.05	38.24	18.52	67.51	-28.90	-28.50
700	56.60	457.1	14.08	37.96	18.64	64.93	-24.90	-36.80
750	56.57	453.9	13.37	38.37	18.20	67.90	-26.80	-45.80
800	56.14	411.1	13.34	38.46	17.68	61.64	-22.50	-46.90
850	56.03	400.9	13.49	38.61	17.42	59.43	-42.90	-46.40
900	56.24	420.7	12.45	38.60	17.64	67.59	-41.70	-31.30
950	56.15	412.1	12.11	39.08	17.07	68.06	-44.10	-35.20
1000	56.31	427.6	13.55	39.05	17.26	63.11	-32.20	-38.40

Applications

- P/L/S band power amplifier
- UHF TV
- Data link power amplifier



Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch-off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	I_{GS}	50.4	mA
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_C = 25^\circ\text{C}$, at $P_{out}=400\text{W}$ @900MHz	$R_{\theta JC}$	0.32	°C /W

Table 3. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

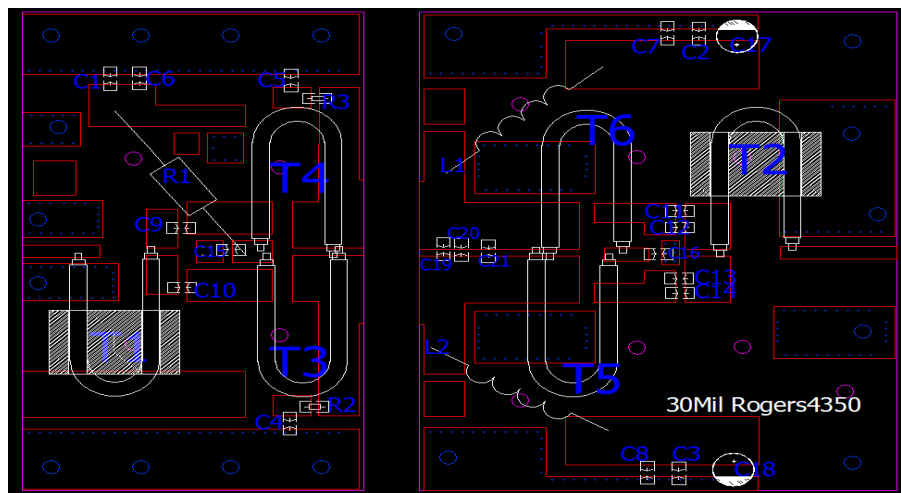
DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 50.4\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 50.4\text{mA}$	$V_{GS(th)}$	-4	-	-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS} = 100\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.2		V

Ruggedness Characteristics

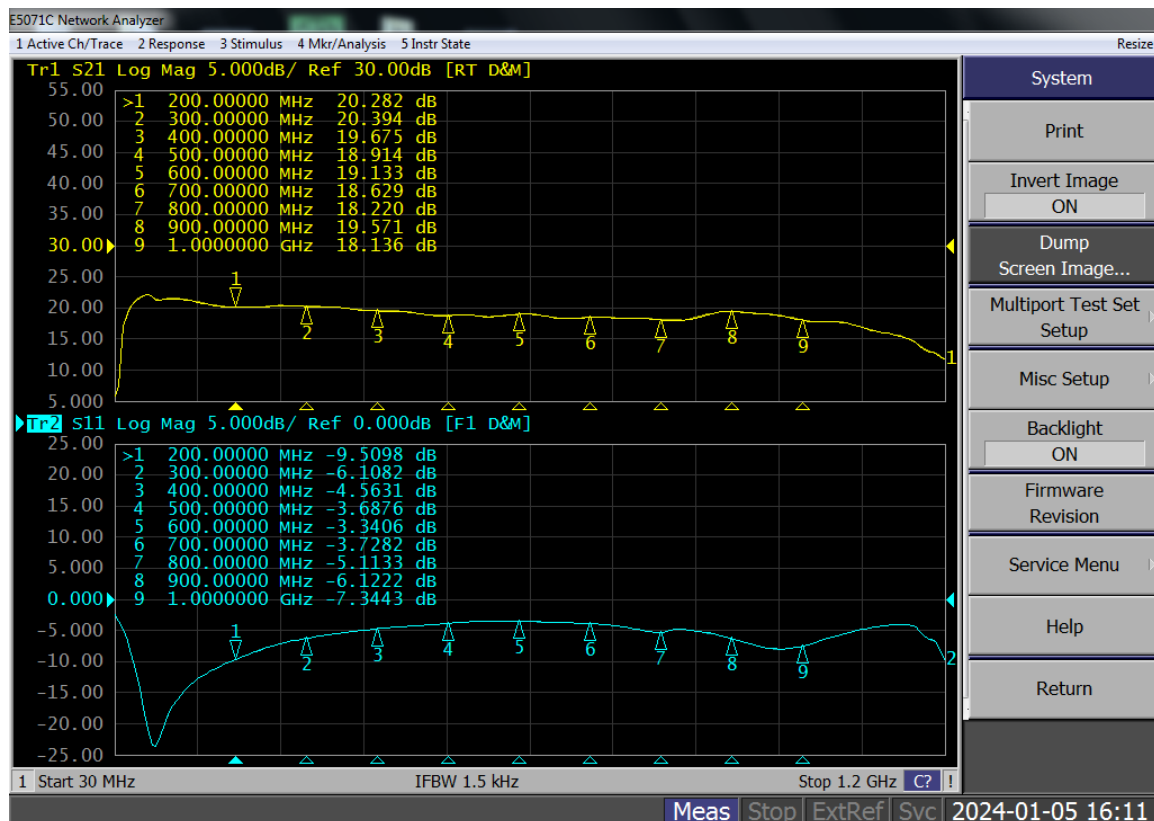
Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	900MHz, $P_{out}=400\text{W}$ pulse CW All phase, No device damages	VSWR		5:1		

Figure 1: Reference design circuit (PCB DWG file upon request,)





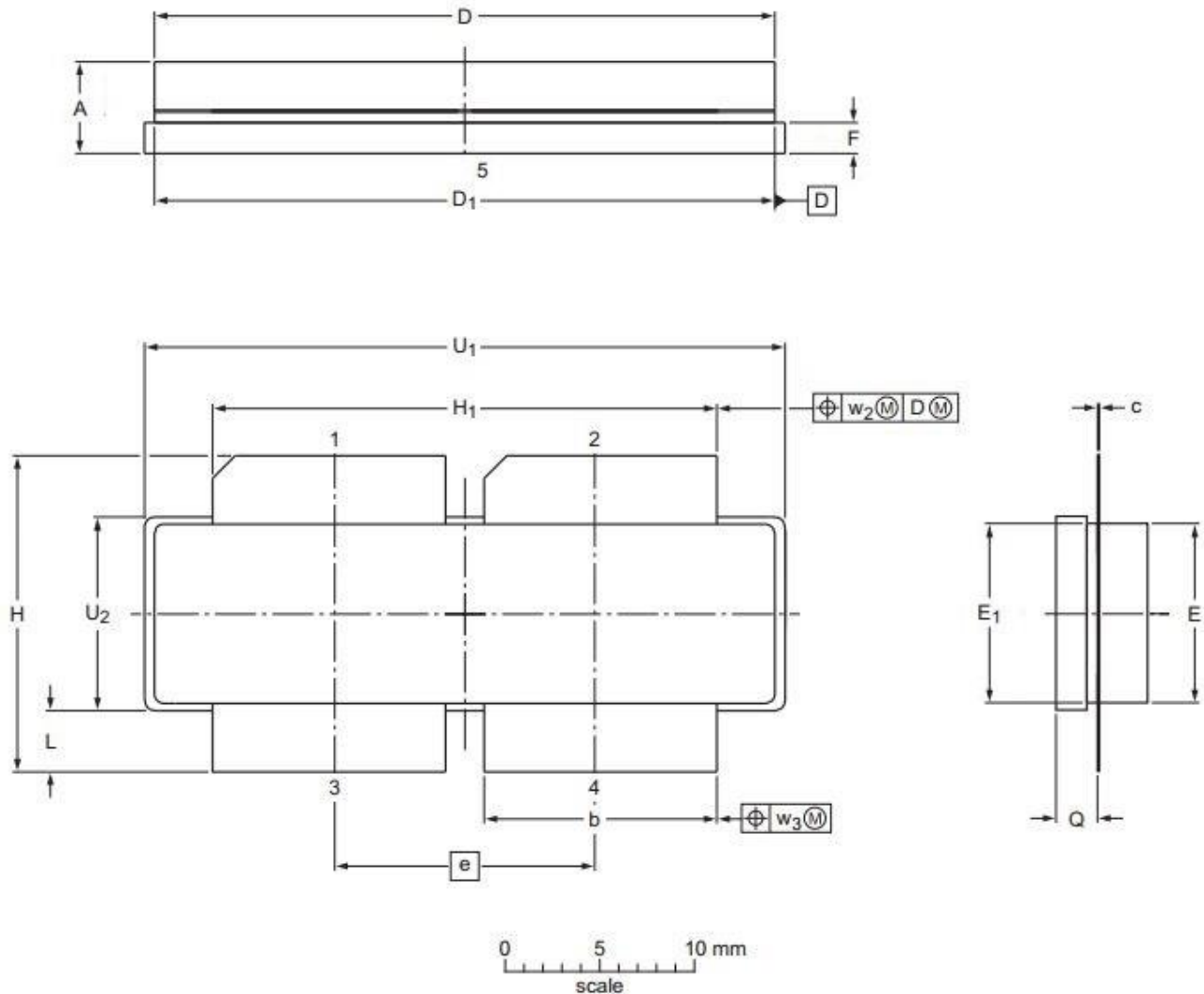
Component	Description	Suggestion
C1~C5	10uF	10uF/100V
C6~C8	200pF	MQ101111
C9,C10	100pF	MQ101111
C11~C14	56pF	MQ101111
C15,C16	560pF	MQ101111
C19	1pF	MQ101111
C20	2pF	MQ101111
C21	8.2pF	MQ101111
C17,C18	1000uF/63V	Electrolytic Capacitor
R1	180 Ω	
R2,R3	10 Ω	Chip Resistor
L1,L2	d=1.5mm, D=5mm, 4 Turns	
T1	50 ohm,60mm	RFSFBUB-086-50,BN-61-202
T2	50 ohm,60mm	RFSFBU-086-50,NXO-60
T3,T4	16.7 ohm,50mm	SFF-16.7-1.5
T5,T6	25 ohm,60mm	SFF-25-1.5
PCB	30Mil Rogers4350	





Package Outline

Earless flanged ceramic package; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₂	W ₂
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2024/1/8	V1.0	Preliminary Datasheet Creation

Application data based on: HL-24-01

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