



160W,50V Plastic RF LDMOS Transistor

ITGV10161C9

Description

The ITGV10161C9 is a dual path 50-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies up to 1GHz, in 12*10mm QFN plastic package, supporting surface mounted on PCB through high density grounding vias.

It can be configured as Doherty to be as high efficiency and low cost driver for 4G/5G application within 0.6-1GHz.



- Typical Doherty RF Performance (On Innegration fixture with device soldered).

$V_{ds}=50V$, $I_{dq}=190mA$ ($V_m=3.4V$, $V_p=2.1V$)

Freq (MHz)	Pout (dBm)	CCDF (dB)	Ppeak (dBm)	Ppeak (W)	ACPR (dBc)	Gain (dB)	Eff (%)
758	43.50	8.69	52.18	165.3	-27.5	17.3	52.4
785	43.50	8.88	52.37	172.5	-28.6	17.8	55.3
803	43.50	8.84	52.33	171.2	-30.4	17.4	51.3

- Typical Doherty RF Performance (On Innegration fixture with device soldered).

$V_{ds}=50V$, $I_{dq}=190mA$ ($V_m=3.4V$, $V_p=2.1V$)

Freq (MHz)	Pout (dBm)	CCDF (dB)	Ppeak (dBm)	Ppeak (W)	ACPR (dBc)	Gain (dB)	Efficiency (%)
578	43.0	8.51	51.52	142.0	-29.5	14.9	42.6
628	43.0	8.32	51.33	135.8	-38.2	15.6	50.3
678	43.0	8.42	51.41	138.5	-33.1	14.7	43.1

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- P band power amplifier
- All 4G/5G cellular application within 0.6 to 1GHz

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C



Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^{\circ}\text{C}$, $T_J = 200^{\circ}\text{C}$, DC test	$R_{\theta JC}$	0.6	$^{\circ}\text{C/W}$

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

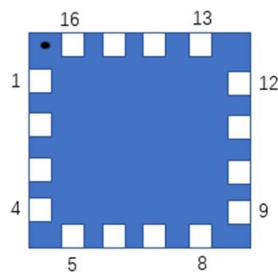
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage $V_{GS} = 0$, $I_{DS} = 100\mu\text{A}$	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 90\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 11\text{V}$, $V_{DS} = 0\text{V}$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 50\text{V}$, $I_D = 600\mu\text{A}$)	$V_{GS(th)}$	—	2	—	V
Gate Quiescent Voltage ($V_{DD} = 50\text{V}$, $I_D = 190\text{mA}$, Measured in Functional Test)	$V_{GS(Q)}$	—	3.4	—	V

Load Mismatch (In Innegration Test Fixture, 50 ohm system): $V_{DD} = 50\text{Vdc}$, $I_{DQ} = 190\text{mA}$, $f = 880\text{MHz}$

VSWR 10:1 at 160W pulse CW Output Power	No Device Degradation
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Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)



Pin No.	Symbol	Description
5,6	RF IN/Vgs of Main	RF Input/Gate bias of main path
7,8	RF IN/Vgs of Peak	RF Input/Gate bias of peak path
13,14	RF OUT/Vds of Peak	RF Output/Drain bias of peak path
15,16	RF OUT/Vds of Main	RF Output/Drain bias of main path
Other Pins	GND	Grounding
Package Base	GND	DC/RF Ground. Proposed to be soldered to heatsink plane directly for the best CW thermal and RF performance. Soldered through vias or copper coin allowed for pulsed CW and back off applications, but will result in higher junction temperatures

758-803MHz application board

Reference Circuit of Test Fixture Assembly Diagram

20mils RO4350B

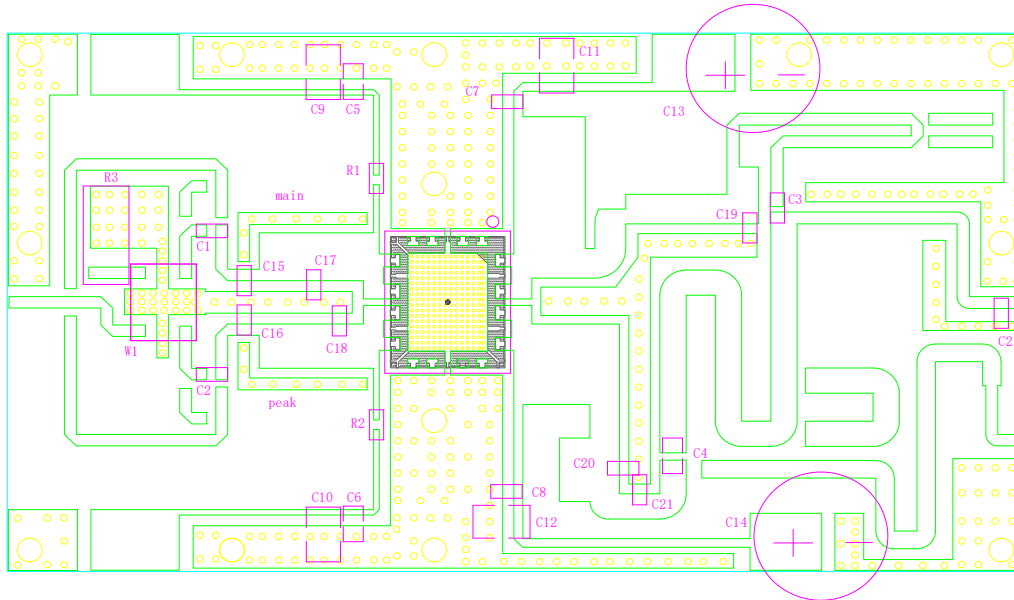


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Designator	Footprint	Comment	Quantity
C1, C2, C4, C5, C6, C7, C8	0603	68 pF	7
C3	0603	8.2 pF	1
C9, C10, C11, C12	1210	10uF/100V	4
C13, C14		220uF/63V	2
C15, C16	0603	12 pF	2
C17	0603	2.7 pF	1
C18, C20, C21	0603	6.8 pF	3
C22	0603	2.2 pF	1
R1, R2	0603	10Ω	2
R3	2512	51Ω	1
W1		DC07F02 (YANTEL 2dB)	1

TYPICAL CHARACTERISTICS

Figure 5. Power Gain and Drain Efficiency as function of Power Output at $I_{dq}=190\text{mA}$

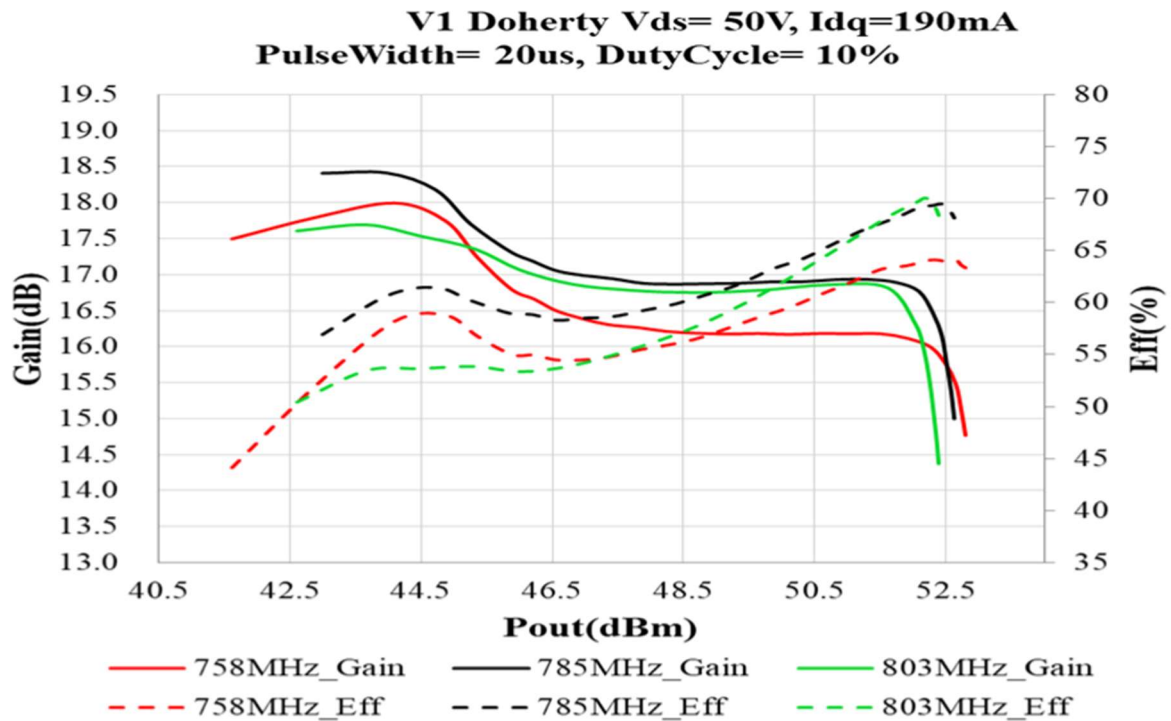
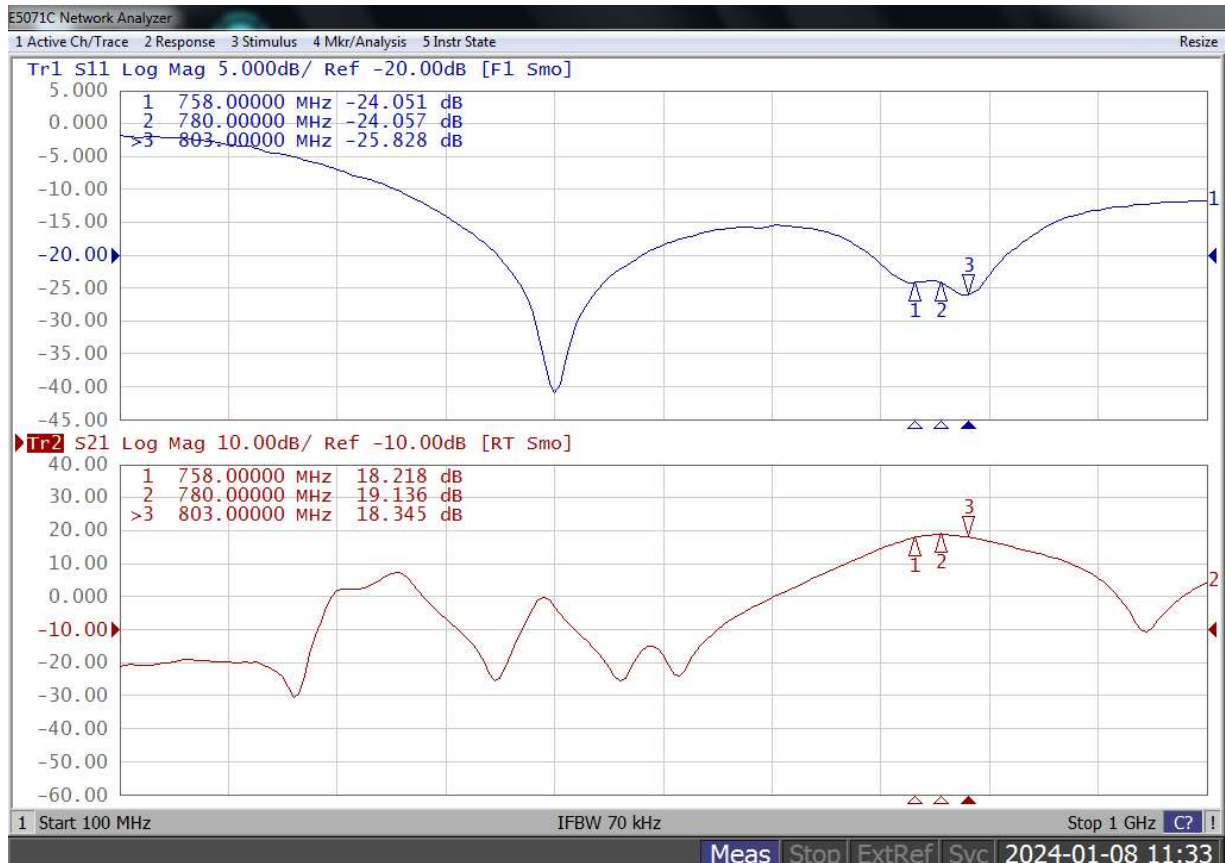


Figure 5. Network analyzer output S11/S21



578-678MHz application board

Reference Circuit of Test Fixture Assembly Diagram 20mils RO4350B

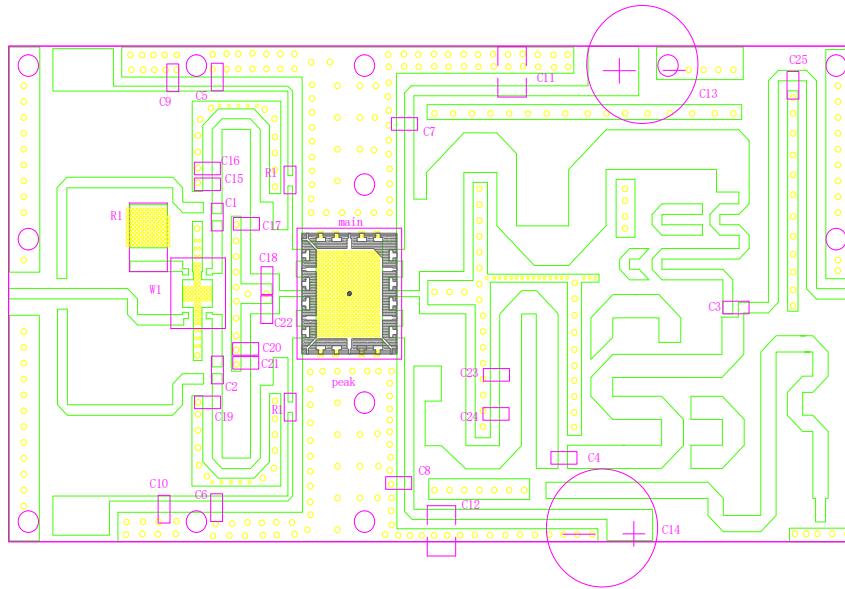


Figure 6. Test Circuit Component Layout

Table 6. Test Circuit Component Designations and Values

Designator	Footprint	Comment	Quantity
C1, C2, C17, C20, C21	0603	15 pF	5
C3, C4, C5, C6, C7, C8	0603	100 pF	6
C9, C10	0603	0.1 uF	2
C11, C12	1210	10uF/100V	2
C13, C14		220uF/63V	2
C16, C25	0603	3.9 pF	2
C18, C22	0603	20 pF	2
C15, C19, C23, C24	0603	6.8 pF	4
R1, R2	0603	10Ω	2
R3	2512	51Ω	1
W1		DC07F02 (YANTEL 2dB)	1

TYPICAL CHARACTERISTICS

Figure 7. Power Gain and Drain Efficiency as function of Power Output at $I_{dq}=190\text{mA}$

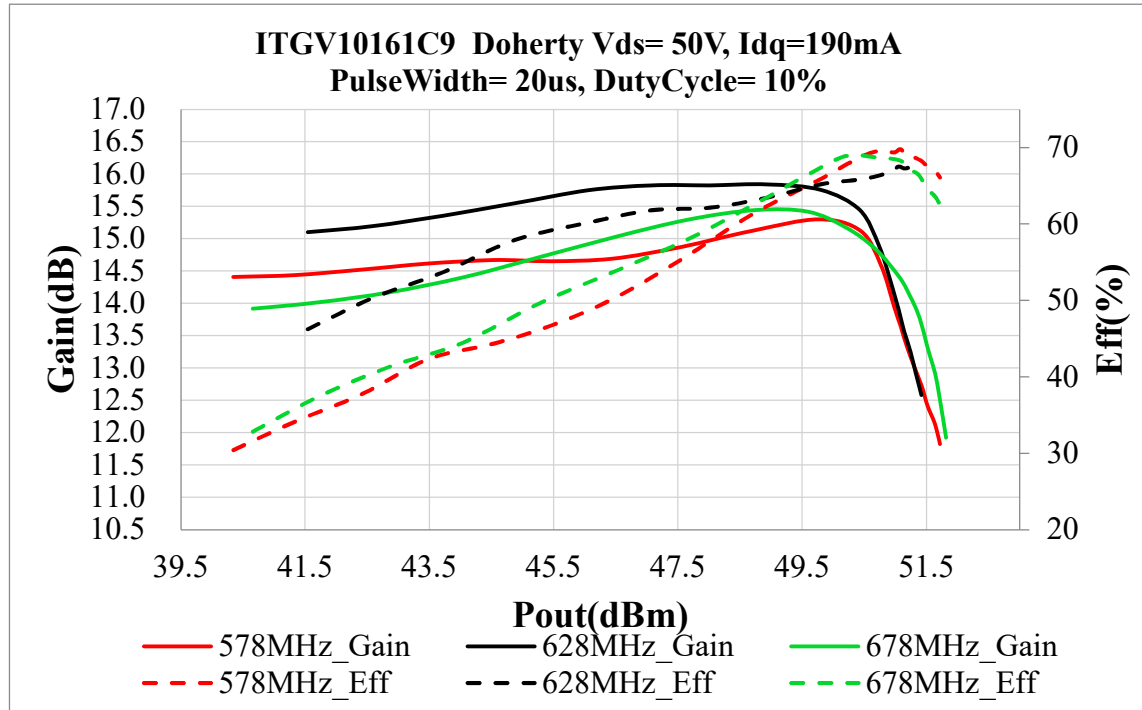
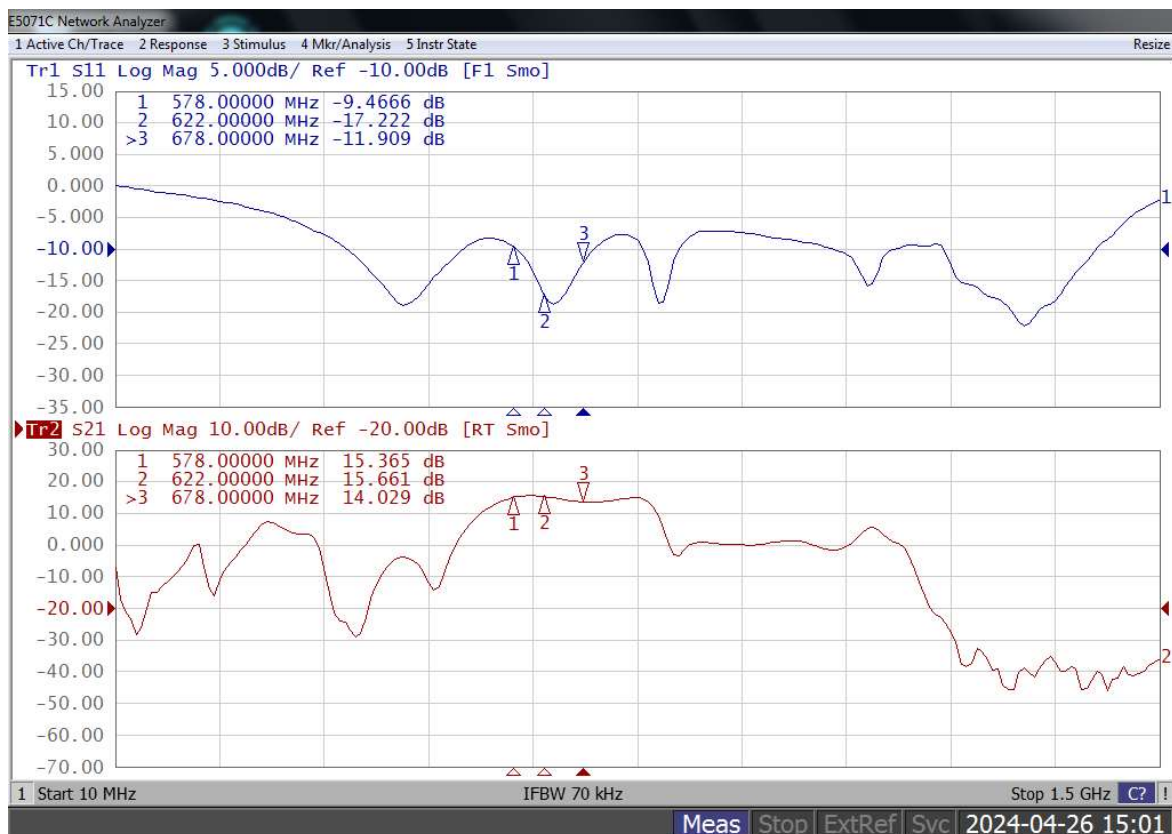
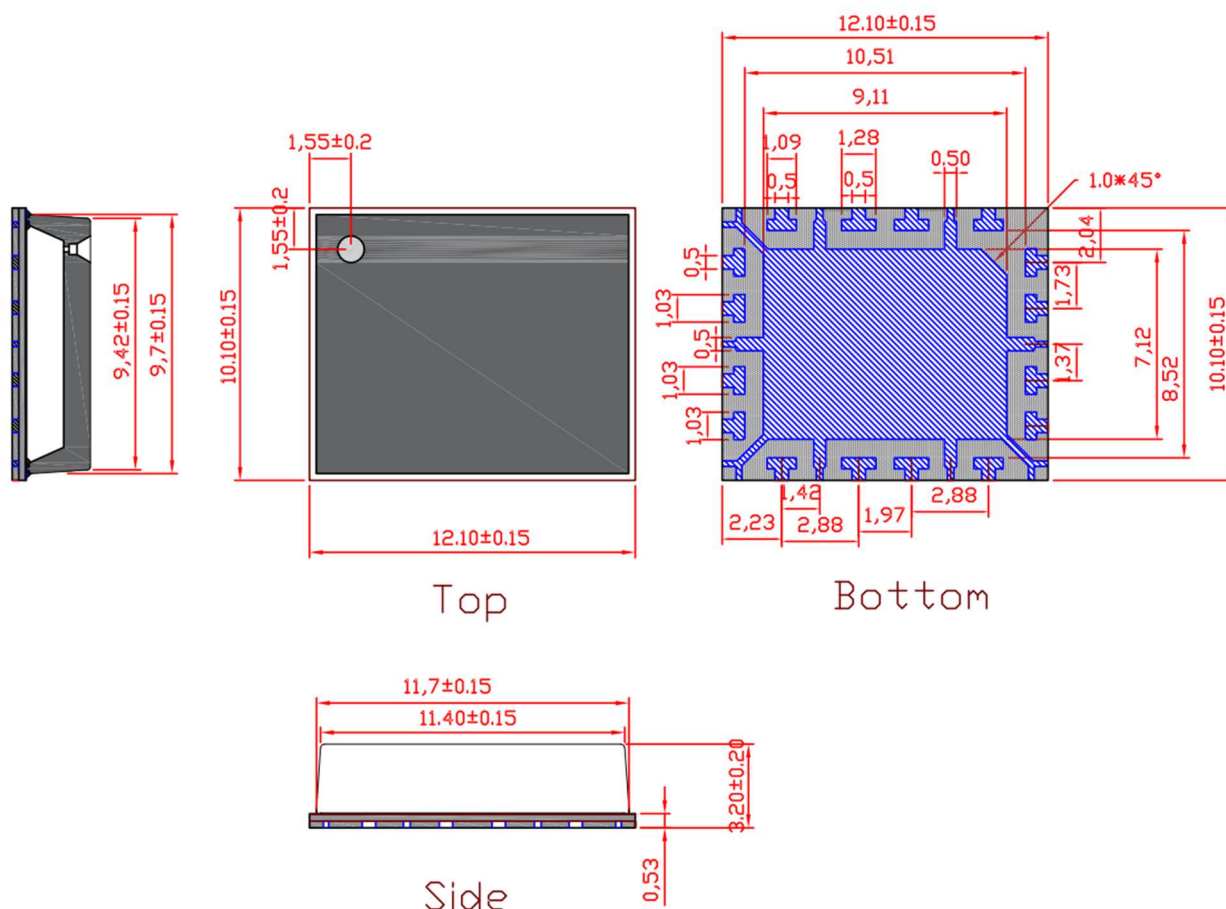


Figure 8. Network analyzer output S11/S21





Package Dimensions (Unit:mm)



Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2024/1/8	Rev 1.0	Preliminary Datasheet
2024/4/26	Rev 1.1	Add 578-678 application data

Application data based on LSM-24-01/14

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