

Document Number: ITGV10200C9 Preliminary Datasheet V1.2

### 200W,50V Plastic RF LDMOS Transistor

### **Description**

The ITGV10200C9 is a dual path 50-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies up to 1GHz, in 12\*10mm QFN plastic package, supporting surface mounted on PCB through high density grounding vias.

It can be configured as Doherty to be as high efficiency and low cost driver for 4G/5G application within 0.6-1GHz.

Typical Doherty RF Performance (On Innogration fixture with device soldered).

Freq	Pout	Psat	ACPR	Gain	Eff
(MHz)	(dBm)	(W)	(dBc)	(dB)	(%)
758-821	45	210	-30	18	52
869-894	45	210	-28	19	52

### **Features**

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCl drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

### **Suitable Applications**

- P band power amplifier
- All 4G/5G cellular application within 0.6 to 1GHz

### **Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
DrainSource Voltage	V <sub>DSS</sub>	+110	Vdc
GateSource Voltage	$V_{GS}$	-10 to +10	Vdc
Operating Voltage	V <sub>DD</sub>	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	Tc	+150	°C
Operating Junction Temperature	T₃	+225	°C

### **Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	Desig	0.55	00/14/
T <sub>C</sub> = 85°C, T <sub>J</sub> =200°C, DC test	R⊕JC	0.55	°C/W

#### **Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22A114)	Class 2

#### Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit	
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#### **DC Characteristics**

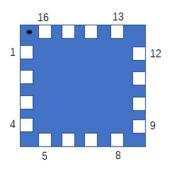
Drain-Source Voltage	\/	110		V
V <sub>GS</sub> =0, I <sub>DS</sub> =100uA	V <sub>(BR)DSS</sub>	110		V
Zero Gate Voltage Drain Leakage Current		 	4	
$(V_{DS} = 90V, V_{GS} = 0 V)$	I <sub>DSS</sub>	 	l I	μΑ
GateSource Leakage Current		 	1	^
$(V_{GS} = 11 \text{ V}, V_{DS} = 0 \text{ V})$	I <sub>GSS</sub>	 	<b>'</b>	μΑ
Gate Threshold Voltage	\/ (#L)	 2		V
$(V_{DS} = 50V, I_D = 600 \mu A)$	V <sub>GS</sub> (th)	 2		V
Gate Quiescent Voltage	\/	3.14		V
(V <sub>DD</sub> = 50V, I <sub>D</sub> = 60mA, Measured in Functional Test)	$V_{GS(Q)}$	 3.14		V

**Load Mismatch (In Innogration Test Fixture, 50 ohm system):**  $V_{DD} = 50 Vdc$ ,  $I_{DQ} = 60 mA$ , f = 800 MHz

VSWR 10:1 at 200W pulse CW Output Power	No Device Degradation
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Figure 1: Pin Connection definition

### Transparent top view (Backside grounding for source)



Pin No.	Symbol	Description
5,6	RF IN/Vgs of Main	RF Input/Gate bias of main path
7,8	RF IN/Vgs of Peak	RF Input/Gate bias of peak path
13,14	RF OUT/Vds of Peak	RF Output/Drain bias of peak path
15,16	RF OUT/Vds of Main	RF Output/Drain bias of main path
Other Pins	GND	Grounding
		DC/RF Ground. Proposed to be soldered to heatsink plane directly for the best CW thermal
Package Base	GND	and RF performance. Soldered through vias or copper coin allowed for pulsed CW and back
		off applications, but will result in higher junction temperatures



### 758-821MHz application board

# Reference Circuit of Test Fixture Assembly Diagram 20mils RO4350B

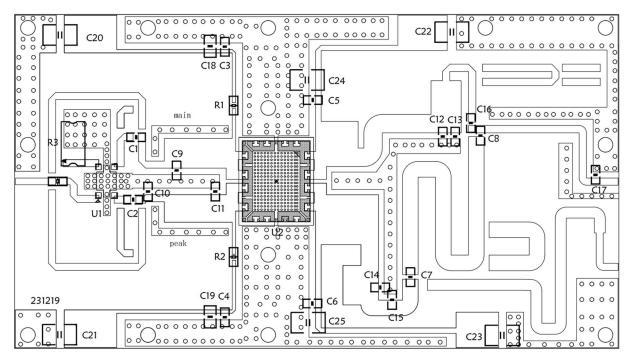


Figure 2. Test Circuit Component Layout

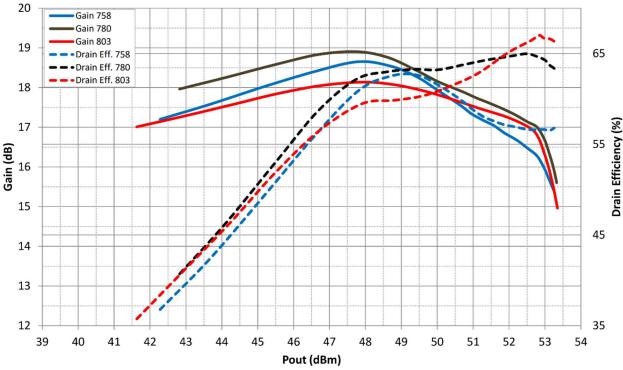
**Table 5. Test Circuit Component Designations and Values** 

Reference	Footprint	Value	Quantity
C1, C2, C3, C4, C5, C6,	0603	68pF/250V	8
C7, C8	0003	υσρι / 230 ν	U
C9, C16	0603	15pF/250V	2
C10	0603	12pF/250V	1
C11, C14, C15	0603	6.8pF/250V	3
C12, C17	0603	3.9pF/250V	2
C13	0603	5.6pF/250V	1
C18, C19	0805	1nF/50V	2
C20, C21, C22, C23,	1210	10uF/100V	6
C24, C25	1210	1007/1007	0
R1, R2	0603	10R	2
R3	2512	51R	1
U1	3.18*5.08mm	X3C07F1-02S	1
U2	C9	ITGV10200C9	1



### TYPICAL CHARACTERISTICS

Figure 5. Power Gain and Drain Efficiency as function of Power Output at Idq=60mA



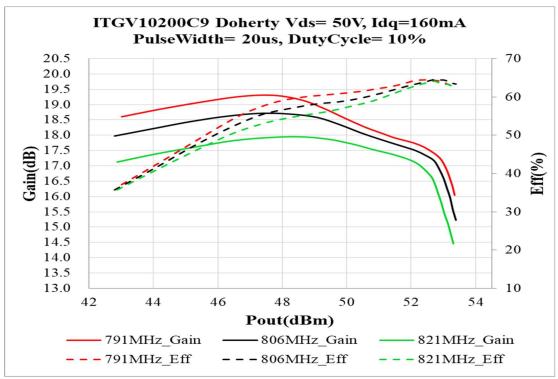
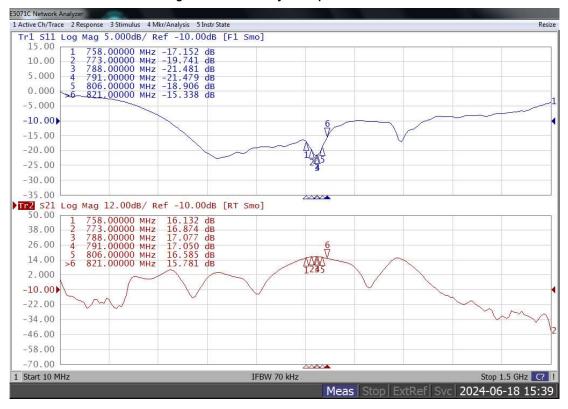


Figure 5.Network analyzer output S11/S21



### 869-894MHz application board

# Reference Circuit of Test Fixture Assembly Diagram 20mils RO4350B

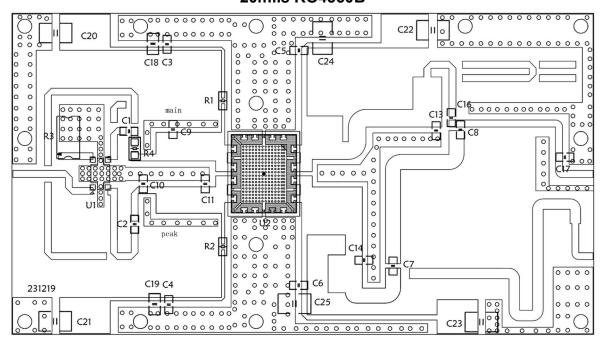


Figure 6. Test Circuit Component Layout

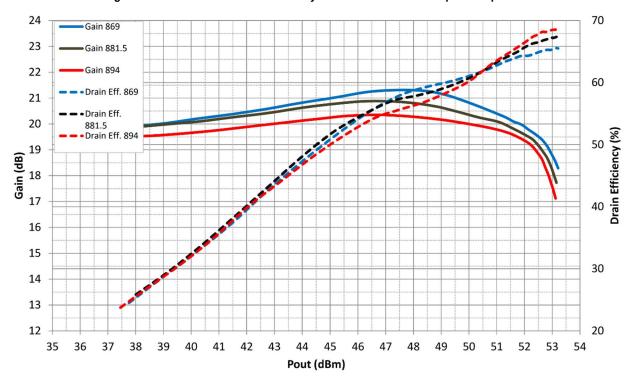


**Table 5. Test Circuit Component Designations and Values** 

Reference	Footprint	Value	Quantity
C2, C3, C4, C5, C6, C7, C8	0603	68pF/250V	7
C1	0603	15pF/250V	1
C9, C14	0603	10pF/250V	2
C10	0603	6.8pF/250V	1
C11	0603	8.2pF/250V	1
C13	0603	5.6pF/250V	1
C16	0603	3.9pF/250V	1
C17	0603	2.2pF/250V	1
C18, C19	0805	1nF/50V	2
C20, C21, C22, C23, C24, C25	1210	10uF/100V	6
R1, R2	0603	10R	2
R3	2512	51R	1
R4	0805	10R	1
U1	3.18*5.08mm	X3C07F1-02S	1
U2	С9	ITGV10200C9	1

### **TYPICAL CHARACTERISTICS**

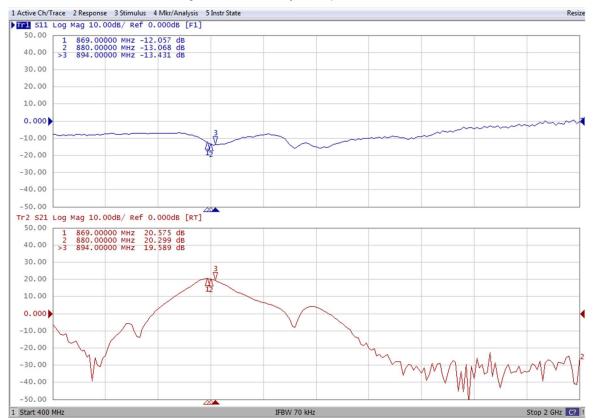
Figure 7. Power Gain and Drain Efficiency as function of Power Output at Idq=60mA





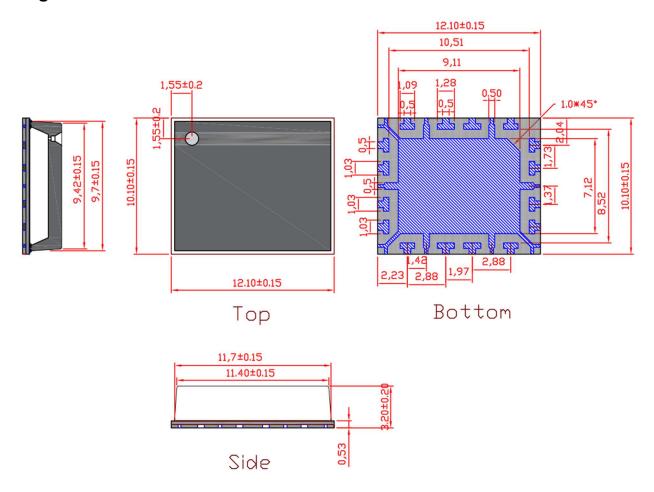
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#### Figure 8.Network analyzer output S11/S21





### Package Dimensions (Unit:mm)



### **Revision history**

Table 7. Document revision history

Date	Revision	Datasheet Status
2024/2/2	Rev 1.0	Preliminary Datasheet
2024/3/4	Rev 1.1	Add 869-894MHz data
2024/6/18	Rev 1.2	Extended test for 758-821MHz

Application data based on ZBB-24-05/07

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