



GaN 50V, 1800W, 700MHz RF Power Transistor

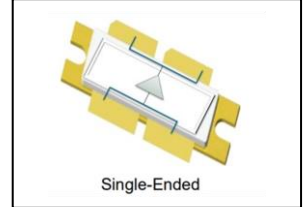
STCV071K8RD4

Description

The STCV071K8RD4 is a 1800W capable, single ended, internally matched GaN HEMT, ideal for ISM or RF energy applications at 915MHz

There is no guarantee of performance when this part is used outside of stated frequencies.

Please notice that both leads at input and output side are internally connected, to configure this device as single ended ,shown as right picture.



- Typical RF performance at 650MHz applications

$V_{ds}=50V$, $V_{gs}=-3.24V$, Pulsed CW, $T_c=25$ degree C

Cooling	Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	Psat Gain(dB)	Psat (dBm)	Psat (W)	Psat Eff(%)
Air	650	61.5	1400	74	17	62.6	1820	82

Recommended driver: ITGV20040J2 (50V LDMOS)

Applications

- 650MHz etc RF Energy
- P band power amplifier
- UHF TV

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically $-5V$
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically $-5V$
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	I_{gs}	234	mA
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_c=25^{\circ}C$, at $P_d=450W$	$R_{\theta JC}$	0.25	°C /W



Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics (measured on wafer prior to packaging)

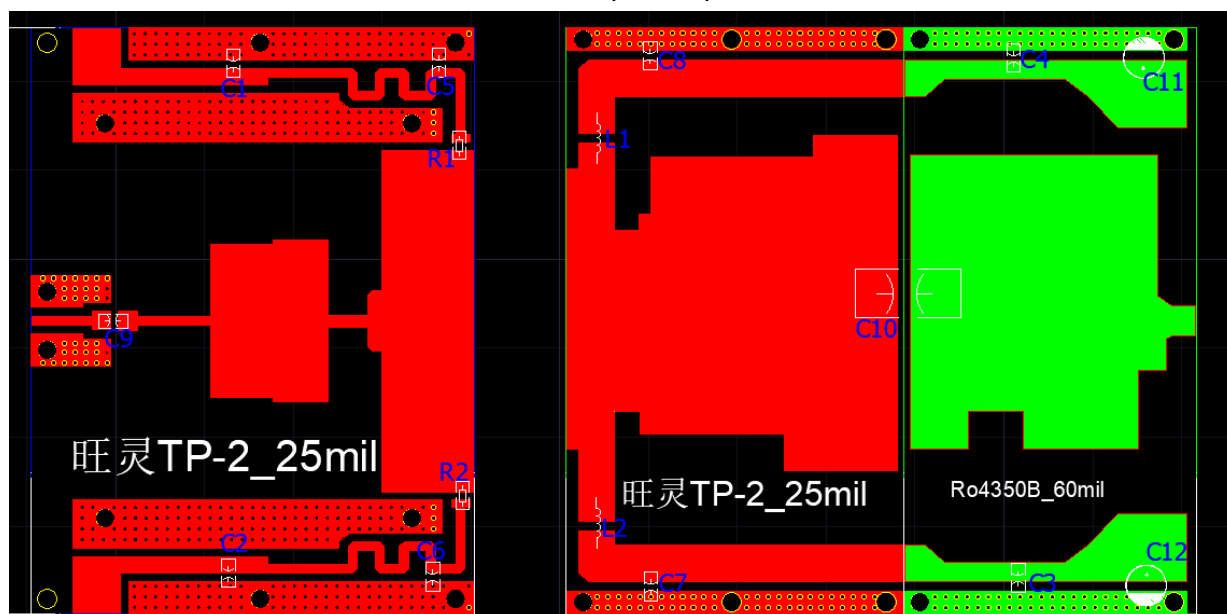
Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=234mA	V _{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID =234mA	V _{GS(th)}	-4	-	-2	V
Gate Quiescent Voltage	VDS =50V, IDS=500mA, Measured in Functional Test	V _{GS(Q)}		-3.1		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	650MHz, Pout=1800W pulse CW All phase, No device damages	VSWR		10:1		

Reference Circuit of Test Fixture Assembly Diagram

DXF file upon request



Component	Description	Suggestion
C1~C4	10uF	10uF/100V
C5~C8	150pF	MQ101111
C9	56pF	MQ101111
C10	75pF	Mica capacitance
C11,C12	4700uF/63V	Electrolytic Capacitor
R1, R2	51 Ω	
L1,L2	d=1.5mm,D=5mm, 3 Turns	
PCB	Wangling TP-2_25mil (ER=6), RED; Ro4350B_60mil, GREEN	



TYPICAL CHARACTERISTICS

Figure 2: S11/S21 output from Network analyser (VDS= 50V, IDQ=500 mA Vgs =-3.1V)

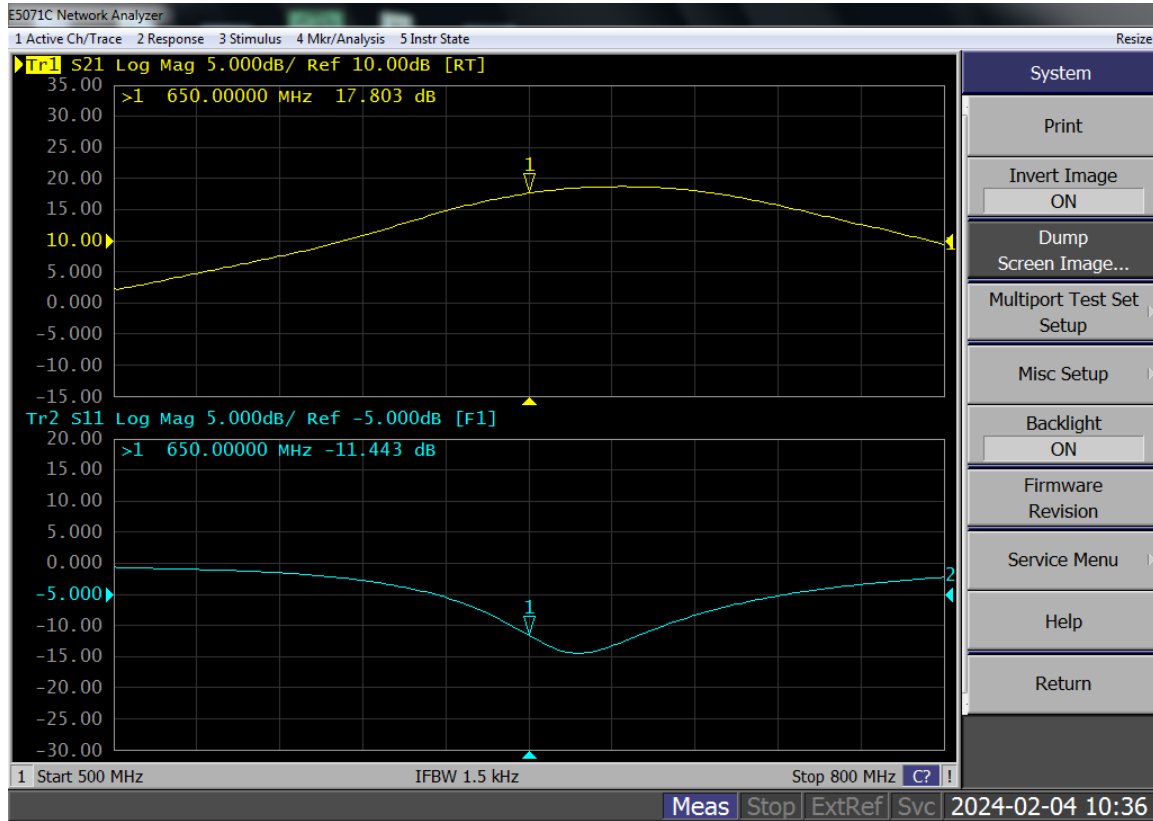
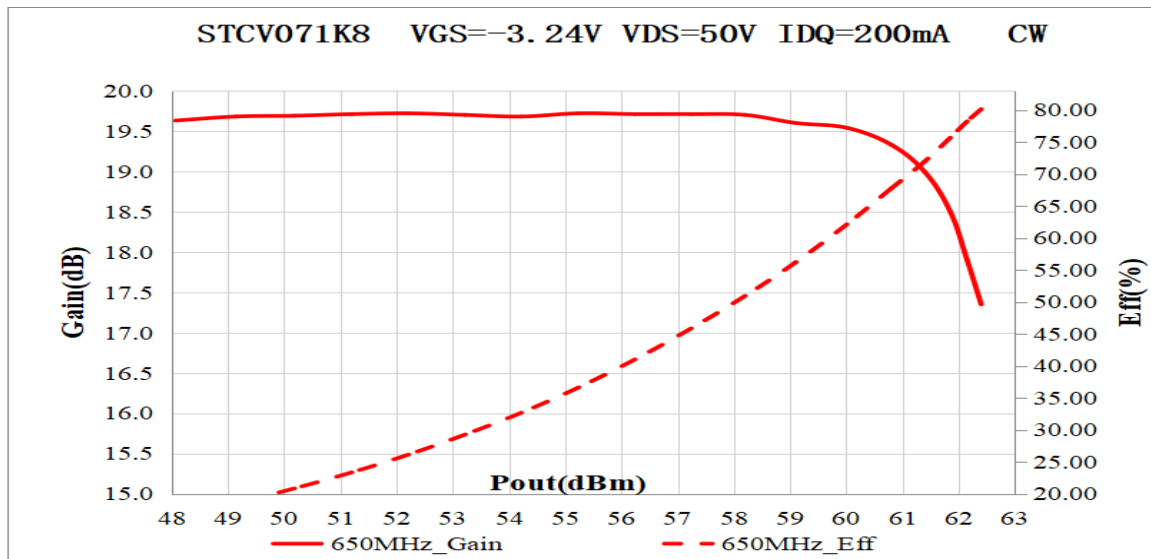


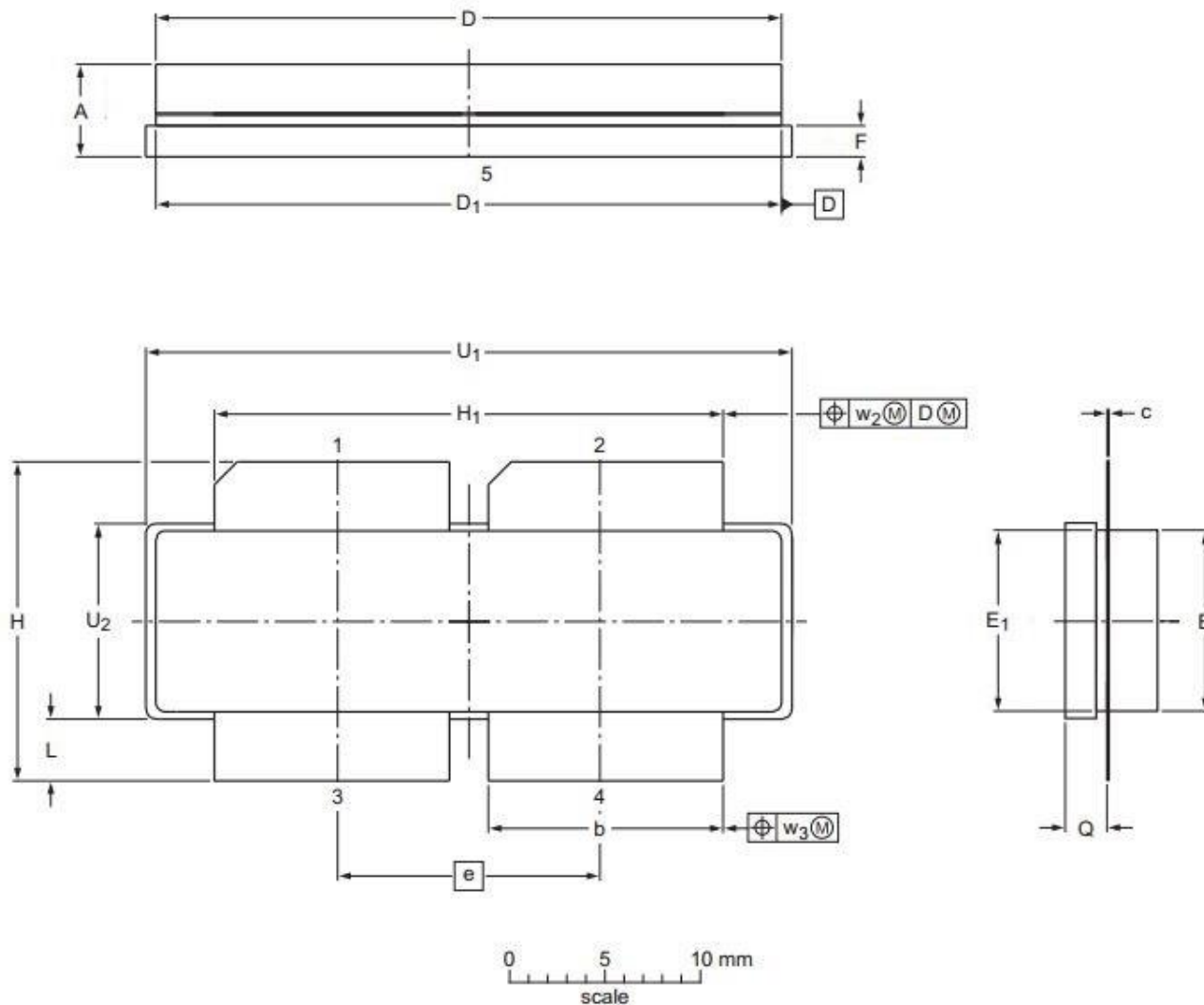
Figure 4: Figure 1: Efficiency and power gain as function of Pout





Package Outline

Earless flanged ceramic package; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₂	W ₂
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2024/2/4	Rev 1.0	Preliminary datasheet creation

Application data based on: TC-24-07

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