



3.3-3.8GHz, 200W, 50V GaN matched PA Module

Description

The SMBV3338-201 is a 200-watt, integrated 2-stage Power Amplifier Module, designed for 5G massive MIMO applications, with frequencies from 3.3 to 3.8 GHz. The module is 50 Ω input fully matched and output partially matched, and requires minimal external components. The module offers a much smaller footprint than traditional discrete component solutions, with much less sensitivity for production, housed in 12*10mm cost effective plastic open cavity package, and heat dissipated by copper flange.

The module incorporates advanced Doherty circuit delivering high power added efficiency for the entire module at 28W average power according to normal 8.5 dB back off.

Innegration owns the patents for internal Doherty architecture, and related plastic open cavity.

- Typical Performance of **3.3-3.8G Full band** Doherty (On Innegration fixture with device soldered on copper coin directly):
VDS=48V, Idq-main=135mA Vgs-main=-3.1V. Vgs-peak=-5.3V, Idq-driver=45mA, Vgs-Driver=-3.14V

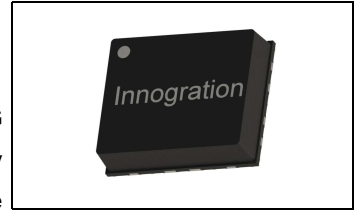
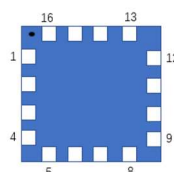
Freq (GHz)	Pulse CW Signal(1)			Pavg=44.5dBm WCDMA Signal(2)		
	P1-Gain (dB)	P5 (dBm)	P5 (W)	Gp (dB)	Eff (%)	ACPR5M (dBc)
3.30	28.93	52.99	199	28.23	43.34	-27.65
3.40	29.62	53.25	211	29.55	41.17	-33.68
3.50	29.59	53.39	218	29.52	40.72	-34.32
3.60	29.51	53.50	224	29.34	41.76	-31.48
3.70	29.16	53.41	219	28.64	42.12	-29.94
3.80	28.78	52.97	198	28.09	41.43	-29.18

Notes: (1)Pulse Width=20 us, Duty cycle=10% (2)WCDMA signal: 3GPP test model 1; 1 to 64 DPCH; Channel Bandwidth=3.84MHz,PAR =10.5 dB at 0.01 % probability on CCDF.

Features and Benefits

- Adjustable drain bias to fit different power demand
- Excellent VBW performance to enable the broadest IBW/OBW
- ✓ Industry leading RF performance for 5G MIMO AAU, for instance: 32T:640W / 400MHz
- Plastic open cavity without molding compound brings advantage compared to molded design
- ✓ Minimize the risk of high density thermal distribution in fanless system for longer life time
- ✓ Highly consistent RF performance for yield of volume production
- 50 Ω Input matched, output partially matched, total effective PCB space smaller than 25*35mm
- Integrated Doherty Final and driver Stage
- 12*10 mm Surface Mount Package, full copper flange underneath for grounding and heat dissipation, much more effective than LGA PCB based design

Pin Configuration and Description (Top view)





Pin No.	Symbol	Description
3	RF IN	RF Input
1	Vds-driver	Driver stage, Drain Bias
2	Vgs-driver	Driver stage, Gate Bias
9,10	RF Out2/Vds-Main	RF Output, Drain Bias of Main Amplifier
11,12	RF Out1/Vds-Peak	RF Output, Drain Bias of Peaking Amplifier
6	Vgs-main	Main Amplifier, Gate Bias
13	VBE-peak	VBW enhancement for Peak
15	Vgs-peak	Peaking Amplifier, Gate Bias
8	VBE-main	VBW enhancement for Main
4,5,7,14,16	NC	No connection
Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.6	Vdc
Operating Voltage	V_{DD}	+60	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance@Average Power, Junction to Case $T_{case}=+85^{\circ}\text{C}$, CW Test, $P_{out}=25\text{W}$,	$R_{\theta JC}$	1.06	°C/W

Notes:

- (1) The thermal resistance is acquired by our company's FEA model, which was calibrated by IR measurement, the value shall be applied to reliability.
- (2) The reference T_{case} temperature 85°C is apply on the backside of package.
- (3) It is recommended to use copper coin underneath to maximize the heat dissipation.
- (4) The power dissipation in the table is overall dissipation which includes Carrier PA, Peaking PA and driver PA..

Table 3. ESD Protection Characteristics

Test Methodology	Class Voltage
Human Body Model(HBM) (JEDEC Standard JESD-A114)	$\pm 200\text{V}$
Charged Device Model (CDM) (JEDEC Standard JESD22-C101F)	$\pm 1000\text{V}$

Table 4. Electrical Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range		3.3		3.8	GHz
Driver Quiescent Current ($I_{DQ-driver}$)			45		mA
Carrier Quiescent Current ($I_{DQ-main}$)			135		mA
Peak PA Gate Quiescent Voltage (V_{PEAK})			-5.3		V
Power Gain @ $P_{out}=44.5\text{dBm}$	Freq=3.6GHz		29		dB



Efficiency @Pout=44.5dBm	Freq=3.6GHz		40		%
Ppeak by CCDF	Freq=3.6GHz		200		W

Load Mismatch of per Section (On Test Fixture, 50 ohm system): $f = 3.6\text{GHz}$

VSWR 10:1 at P3dB pulse CW Output Power	No Device Degradation
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TYPICAL CHARACTERISTICS

Figure 1. Power Gain and Drain Efficiency as Function of Pulsed CW Output Power @VDS=48V

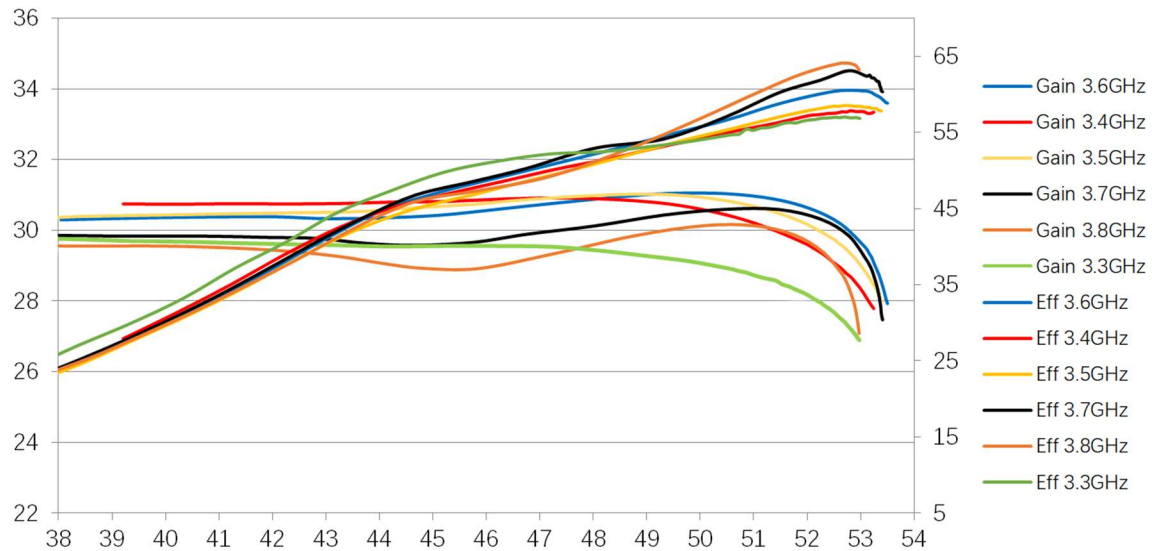


Figure 2. Network analyzer output S11/S21

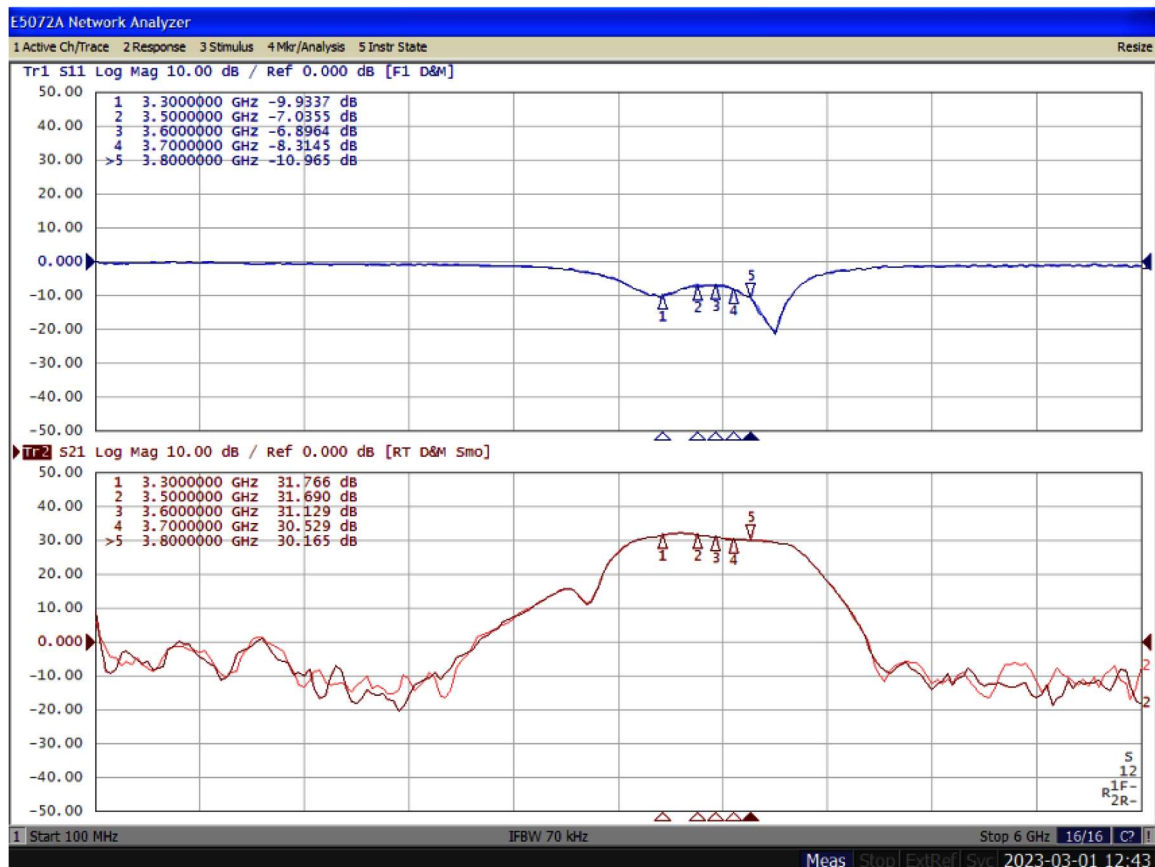


Figure 3: Picture of application board Doherty circuit for 3.4-3.8GHz

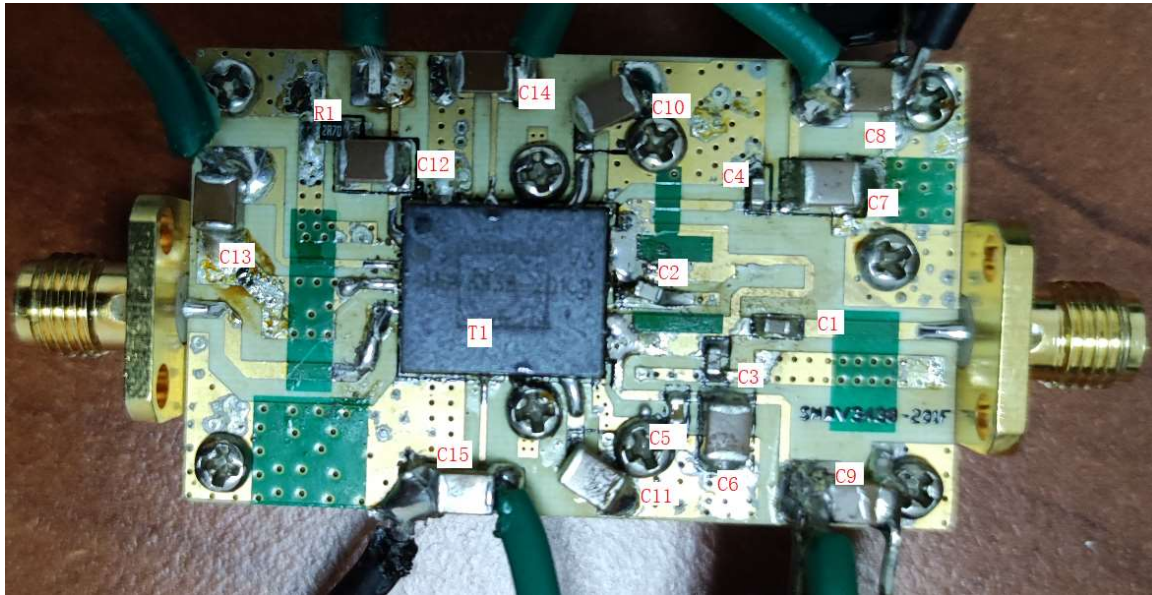
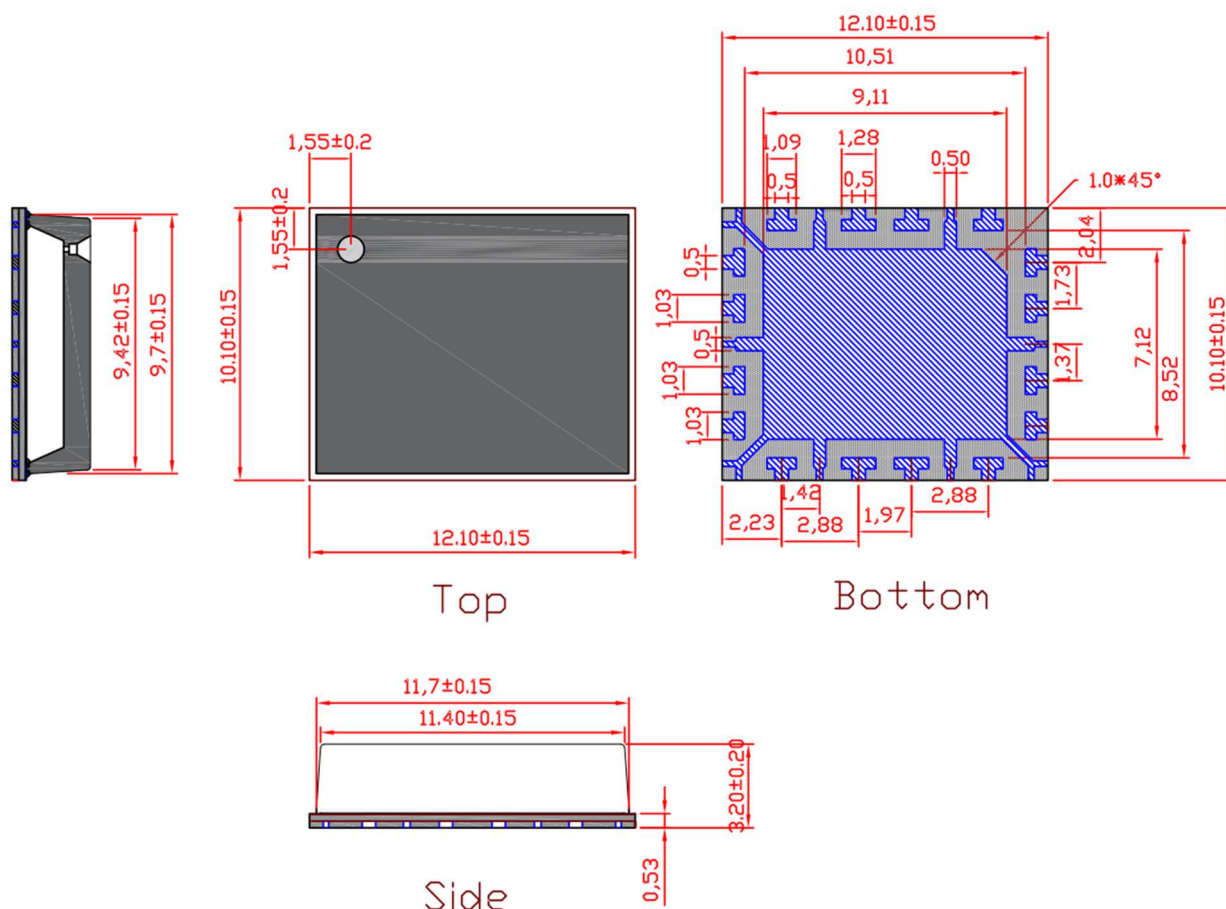


Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

Test Board Bom				
Part	Quantity	Description	Part Number	Manufacture
C1,C4,C5	3	8.2pF High Q Capacitor	251SHS8R2BSE	TEMEX
C2	1	0.6pF High Q Capacitor	251SHS0R6BSE	TEMEX
C3	1	0.4pF High Q Capacitor	251SHS0R4BSE	TEMEX
C6,C7,C8,C9,C10,C11,C12,C13,C14,C15	7	10uF MLCC	RS80R2A106M	MARUWA
R1	1	2.7 Ω Power Resistor	ESR03EZPF2R70	ROHM
T1	1	200W MCM	SMBV3338-201	Innogrations

Package Dimensions



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/3/14	Rev 1.0	Preliminary Datasheet

Application data based on LWH-23-06

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