

M2K1032RVS LDMOS TRANSISTORS

Document Number: M2K1032RVS
Preliminary Datasheet V1.1

320W, 0.7GHz 50V High Power RF LDMOS FETs

Description

The M2K1032RVS is a 320watt capable, high performance, thermally enhanced, unmatched, single ended LDMOS FET, used for any frequency up to 0.7GHz, capable of delivery either CW or pulsed signal.

It is featured with high breakdown voltage and stability, and leading RF performance.



- Typical performance(on 500MHz narrow band application board with devices soldered)

M2K1032RVS Vgs=3.16V Vds=50V Idq=200mA CW								
Freq(MHz)	Pout(dBm)	Pout(W)	IDS(A)	Pin(dBm)	Gain(dB)	Eff(%)	2th(dBc)	3th(dBc)
500	55.45	350.75	9.4	38.5	16.95	74.63	-20.5	-55.2
500	55.3	338.84	9.2	37.5	17.8	73.66	/	/
500	55.1	323.59	8.76	36.5	18.6	73.88	/	/
500	54.9	309.03	8.51	35.5	19.4	72.63	/	/
500	54.51	282.49	8.1	34.5	20.01	69.75	/	/
500	54.2	263.03	7.67	33.5	20.7	68.59	/	/
500	53.81	240.44	7.22	32.5	21.31	66.60	/	/
500	53.3	213.80	6.68	31.5	21.8	64.01	/	/
500	52.6	181.97	6.09	30.5	22.1	59.76	/	/

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	115	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+55	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

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Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 85°C, 320W CW, 50 Vdc, Idq = 200 mA	Rth	0.21	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Drain-Source Voltage VGS=0V, IDS=1.0mA	V _{(BR)DSS}		115		V
Zero Gate Voltage Drain Leakage Current (VDS = 50V, VGS = 0 V)	I _{DSS}	—	—	1	μA
Gate—Source Leakage Current (VGS = 10 V, VDS = 0 V)	I _{GSS}	—	—	1	μA
Gate Threshold Voltage (VDS = 50V, ID = 600 μA)	V _{GS(th)}	—	2.54	—	V
Gate Quiescent Voltage (VDD = 50 V, ID = 200 mA, Measured in Functional Test)	V _{GS(Q)}	—	3.16	—	V
Drain source on state resistance (VDS = 0.1V, VGS = 10 V) Each section side of device measured	R _{ds(on)}		70		mΩ
Common Source Input Capacitance (VGS = 0V, VDS =50 V, f = 1 MHz) Each section side of device measured	C _{ISS}		170		pF
Common Source Output Capacitance (VGS = 0V, VDS =50 V, f = 1 MHz) Each section side of device measured	C _{OSS}		70		pF
Common Source Feedback Capacitance (VGS = 0V, VDS =50 V, f = 1 MHz) Each section side of device measured	C _{RSS}		2		pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): VDD = 50 Vdc, IDQ = 200 mA, f = 500MHz, pulse width:100us, duty

cycle:10%

10:1 at 320W Pulsed CW Output Power	No Device Degradation
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Reference Circuit of Test Fixture (500MHz CW Power Amplifier)

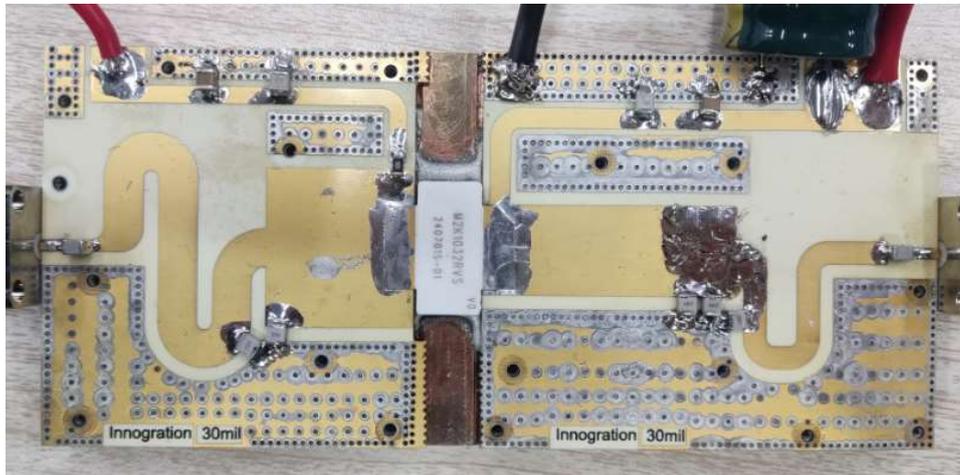
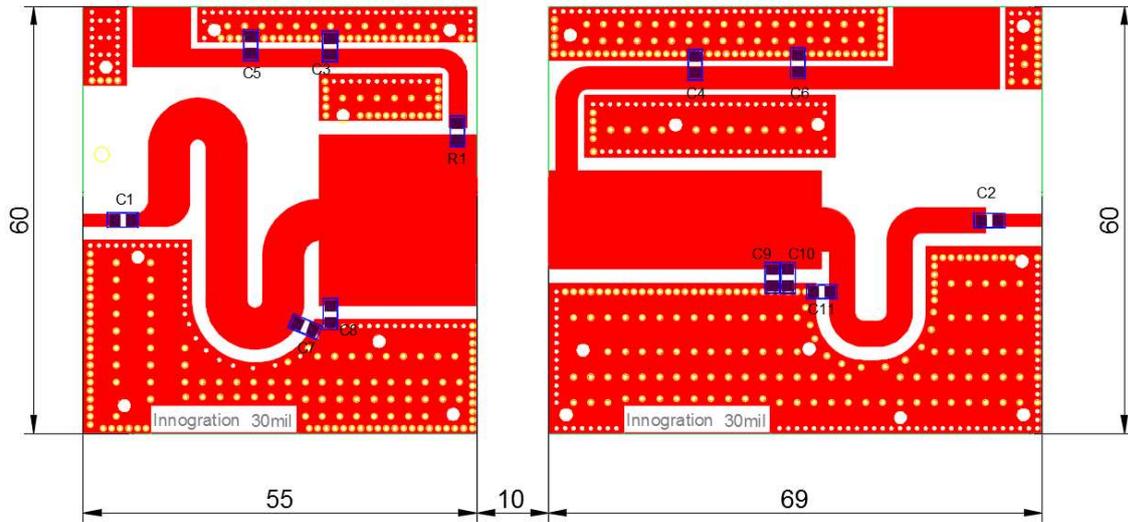
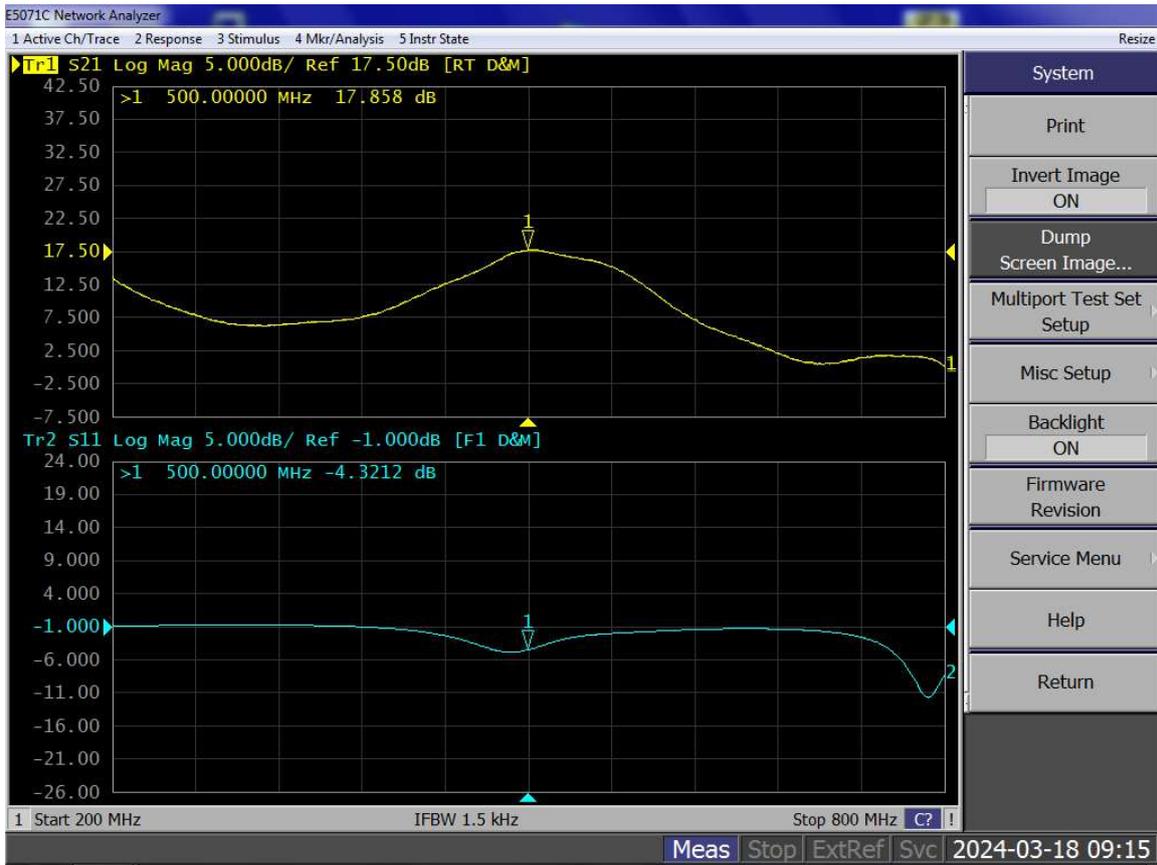


Table 5. Test Circuit Component Designations and Values

Part	Description	Model
C1~C4	820pF MQ101111	
C5,C6	10uF	Ceramic multilayer capacitor
C7	22pF MQ301111	
C8	20pF MQ301111	
C9,C10	4.7pF MQ301111	
C11	18pF MQ301111	
R1	10 Ω 1206	Chip Resistor

Figure 1: Network analyzer output S11/S21, Vds=50V, Idq=200mA

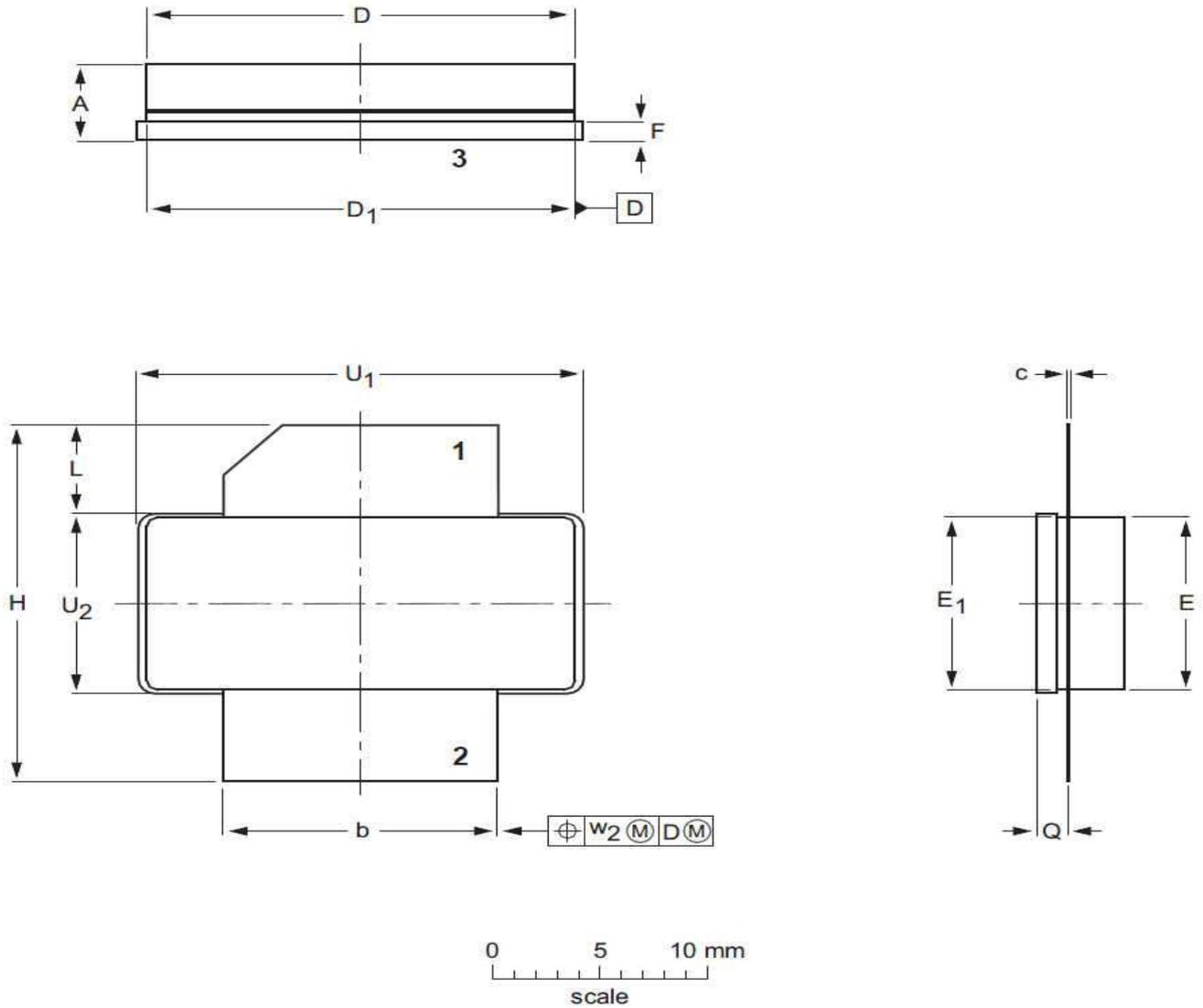


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Package Outline

Earless flanged ceramic package; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	Q	U ₁	U ₂	W ₂
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2024/3/18	Rev 1.0	Preliminary datasheet

Application data based on HL-24-10

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