



0.1-1.0GHz, 10W, 50V LDMOS 2-stage Fully matched PA Module

Description

The I2MGV0110-10 is a 10-watt, 2-stage integrated Power Amplifier Module, designed for broadband applications, with frequencies from 0.1 to 1.0GHz. The module is 50 Ω input/output matched and requires minimal external components.

When used at 28V ,it can enable >5W CW across the same band

The module implements distributed power amplifier in form of multi chips, housed in cost effective plastic open cavity package, offers a much lower cost than traditional MMIC solutions.



Vds=50V, IDQ1=20 mA, IDQ2=60 mA, Pulsed CW 20us, 10%

Parameter	100MHz	300MHz	500MHz	800MHz	1000MHz	1200MHz	Units
Linear Gain	19.7	18.9	18.1	18.3	18.2	17.5	dB
Gain@Pin=24dBm	18.3	17.9	17.1	16.5	16.1	15.4	dB
Pout@Pin=24dBm	17.0	15.4	12.9	11.2	10.2	8.6	W
Eff@Pin=24dBm	39	36	29	25	24	20	%

Vds=28V IDQ1=20 mA, IDQ2=60 mA, CW

Parameter	150MHz	200MHz	400MHz	600MHz	800MHz	1000MHz	Units
Linear Gain	20.0	19.7	18.6	17.6	18.2	17.8	dB
Gain@Pin=23dBm	17.1	17.0	16.5	15.6	15.5	14.8	dB
Pout@Pin=23dBm	10.2	10.0	9.0	7.3	7.0	6.1	W
Eff@Pin=23dBm	53	51	45	35	34	30	%

Product Features

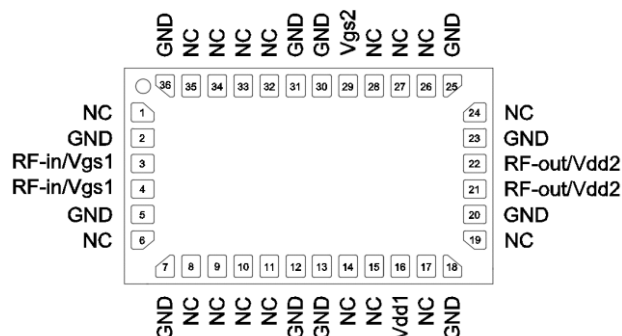
- Operating Frequency Range: 0.1-1.0GHz
- Operating Drain Voltage: +50 V
- 50 Ω Input/Output
- Psat: ≥ 10 W(Pulse)
- Small signal gain:>18dB
- Minimum efficiency:>20%
- 6x10 mm Surface Mount Package
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC
- Much lower cost than GaN-based ultrawide band PA , due to LDMOS technology used

Applications

- Ultra Broadband Amplifiers
- Driver for ISM, FM
- Test Instrumentation
- EMC Amplifier Drivers
- HF/VHF 2-way Radios



Pin Configuration and Description



Pin No.	Symbol	Description
21,22	RFout/Vdd2	Transistor 1, Drain Bias2 & RF Output
3,4	RFin/Vgs1	Transistor 1, Gate Bias1 & RF Input
29	Vgs2	Transistor 1, Gate Bias2
16	Vdd1	Transistor 1, Drain Bias1
Others	NC	No connection
2,5,7,12, 13,18,20,23,25, 30, 31,36 Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+50	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c = 25^\circ\text{C}$, Pulsed CW $P_{out}=10\text{W}@0.5\text{GHz}$	$R_{\theta JC}$	2.8	°C/W

Table 3. Electrical Characteristics

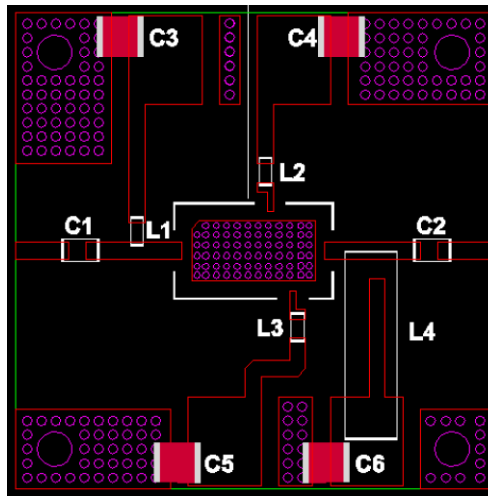
Parameter	Condition	Min	Typ	Max	Unit
Frequency Range	$P_{in}=24\text{dBm}$	100		1000	MHz
Power Gain @ P_{sat}	$P_{in}=24\text{dBm}$	15			dB
P_{SAT}	$P_{in}=24\text{dBm}$	40			dBm
Drain Efficiency @ P_{SAT}	$P_{in}=24\text{dBm}$	20			%

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_{DD} = 50\text{ V}$, Pulse Width=20 us, Duty cycle=10%

Load Mismatch of per Section (On Test Fixture, 50 ohm system): $V_{DD} = 50\text{ V}$, $I_{DQ1+2} = 20+60\text{ mA}$, $f = 0.5\text{GHz}$

VSWR 10:1 at P_{sat} pulse CW Output Power	No Device Degradation
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Reference Circuit of Test Fixture Assembly Diagram



		Part NO.	Vendor
C1, C2	50V 1uF Chip Capacitor	GRM21BR71H105KA12L	muRata
C3,C4,C5,C6	10uF 100V Chip Capacitor	C5750X7S2A106M230KB	TDK
L1, L2,L3	100 nH Capacitor(0603)	LQW18CNR10K00D	muRata
L4	1.3uH 4.2A Inductor	4310LC-132KEC	Coilcraft
PCB	RO4350B,20mil,er=3.48		

TYPICAL CHARACTERISTICS

Figure 1. Network analyzer output S11/S21 (Pin=0dBm) @50V

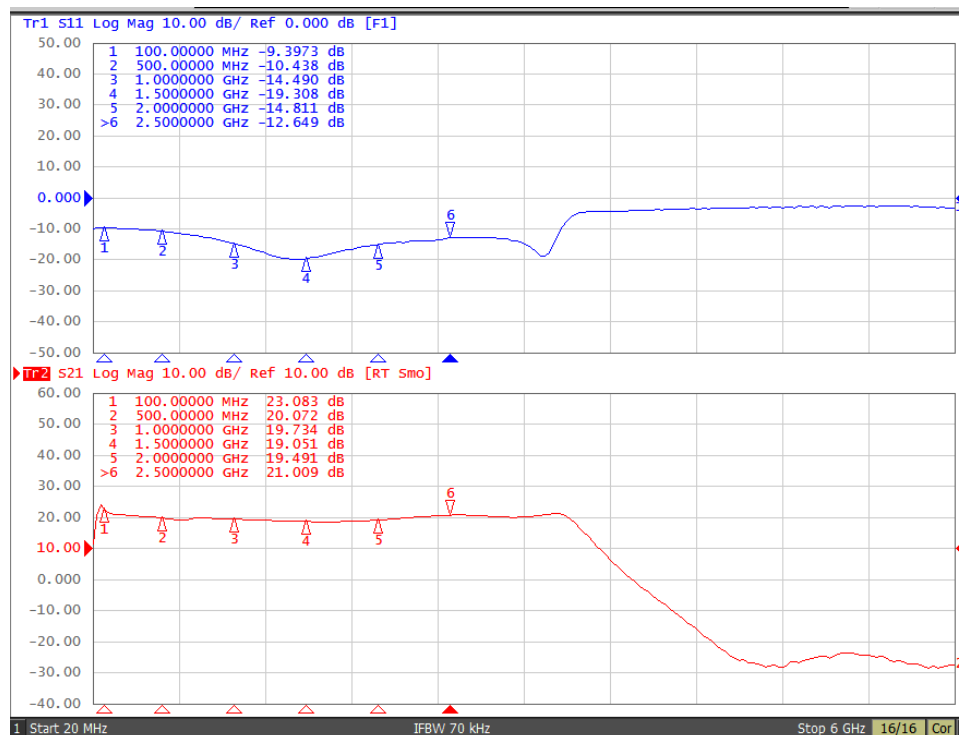
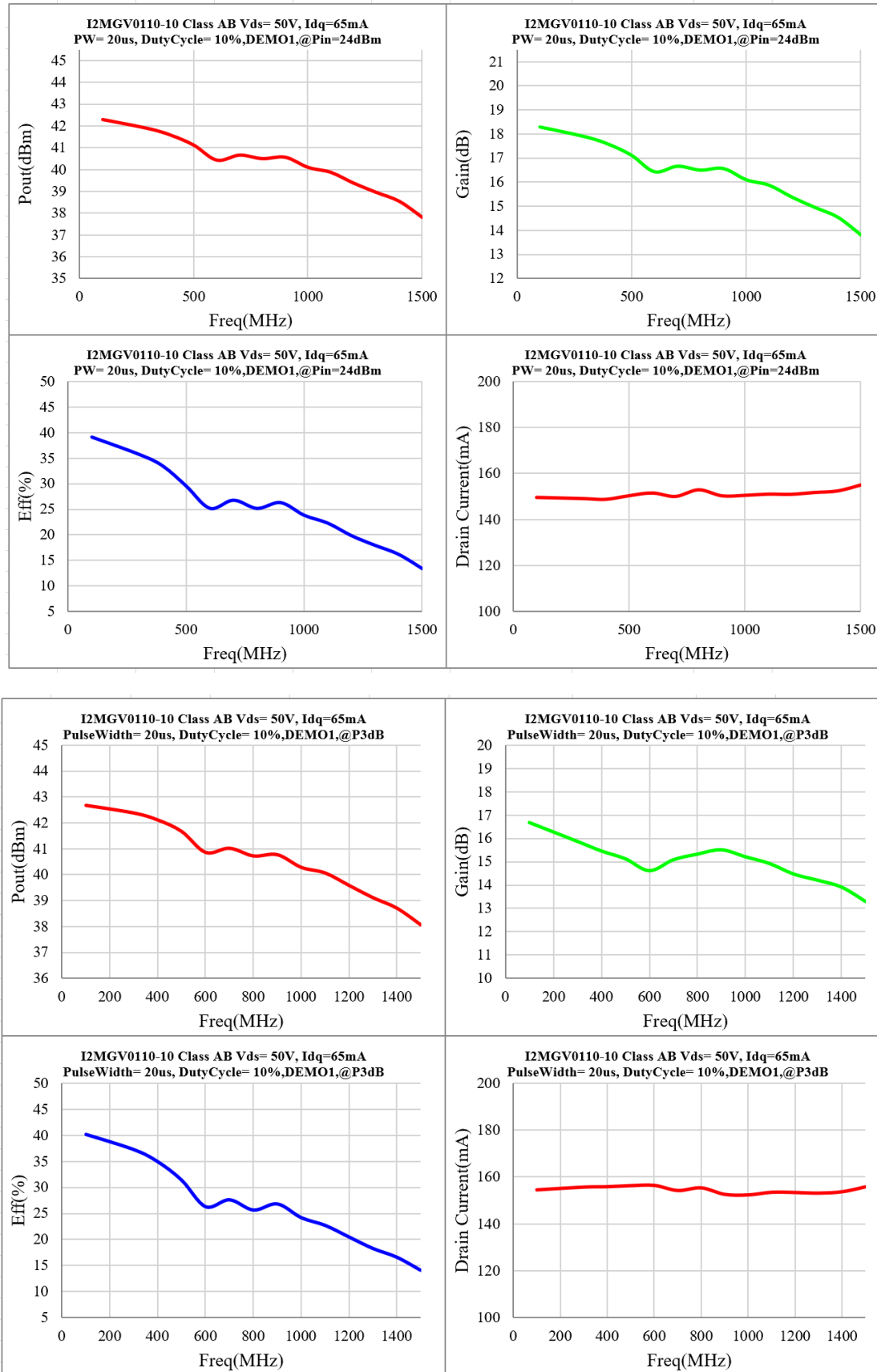


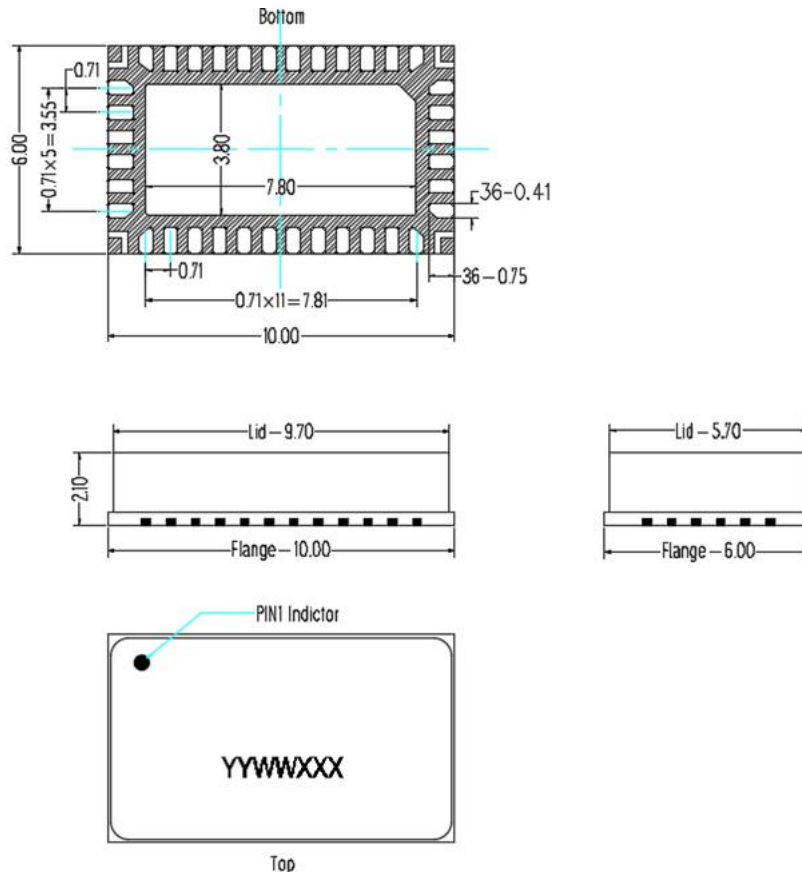


Figure. Power Gain and, efficiency and Pout @Pin=24dBm Pulsed CW ,and P3dB vs. Frequency @50V



Package Dimensions

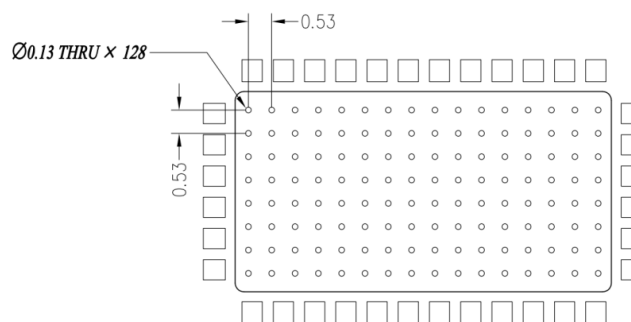
10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ± 0.2 mm.

Mounting Footprint Pattern



Notes:

1. All dimensions are in mm;
2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. ALL vias are PTH to ground.



Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2023/7/3	Rev 1.0	Production Datasheet
2024/3/18	Rev 1.1	Add 28V CW data
2025/5/19	Rev 2.0	Modify the PCB layout by split of Vgs1 and Vgs2

Application data based on ZHH-23-11

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