

# MV0520X LDMOS TRANSISTOR

Document Number: MV0520X  
Preliminary Datasheet V1.1

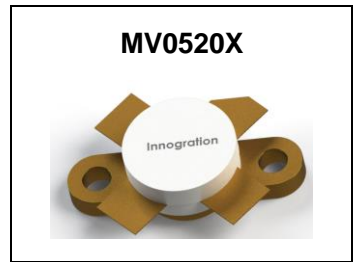
## 200W, HF-200MHz 28V High Power RF LDMOS

### Description

The MV0520X is a 200W single ended 28V LDMOS, highly rugged, unmatched for any applications within HF-200MHz

It supports CW, and pulsed and any modulated signal at either saturated or linear application.

**It is also intended to be the drop-in replacement of legacy VDMOS such as D1017UK etc in the same mechanical outline while with improved performance**



•Typical Performance (On Innogration fixture with device soldered):

$V_{DD} = 28$  Volts,  $I_{DQ} = 150$  mA, CW.

Frequency	Pin (dBm)	Gp (dB)	$P_{OUT}$ (W)	$\eta_D$ (%)
40.68MHz	33	20	203	81

### Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

### Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DS}$	+95	Vdc
Gate--Source Voltage	$V_{GS}$	-10 to +10	Vdc
Operating Voltage	$V_{DD}$	+36	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_c$	+150	°C
Operating Junction Temperature	$T_J$	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^\circ\text{C}$ , $T_J = 200^\circ\text{C}$ , DC test	$R_{\theta JC}$	0.55	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

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**Table 4. Electrical Characteristics** (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>DC Characteristics</b>					
Drain-Source Voltage V <sub>GS</sub> =0, I <sub>DS</sub> =1.0mA	V <sub>(BR)DSS</sub>	95	—		V
Zero Gate Voltage Drain Leakage Current (V <sub>DS</sub> = 75V, V <sub>GS</sub> = 0 V)	I <sub>loss</sub>	—	—	1	μA
Zero Gate Voltage Drain Leakage Current (V <sub>DS</sub> = 28 V, V <sub>GS</sub> = 0 V)	I <sub>loss</sub>	—	—	1	μA
Gate--Source Leakage Current (V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 0 V)	I <sub>gss</sub>	—	—	1	μA
Gate Threshold Voltage (V <sub>DS</sub> = 28V, I <sub>D</sub> = 400 μA)	V <sub>GS(th)</sub>	—	2.2	—	V
Gate Quiescent Voltage (V <sub>DD</sub> = 28 V, I <sub>D</sub> = 150 mA, Measured in Functional Test)	V <sub>GS(Q)</sub>	—	3.05	—	V
Common Source Input Capacitance (V <sub>GS</sub> = 0V, V <sub>DS</sub> =28 V, f = 1 MHz)	C <sub>ISS</sub>		187		pF
Common Source Output Capacitance (V <sub>GS</sub> = 0V, V <sub>DS</sub> =28 V, f = 1 MHz)	C <sub>OSS</sub>		79		pF
Common Source Feedback Capacitance (V <sub>GS</sub> = 0V, V <sub>DS</sub> =28 V, f = 1 MHz)	C <sub>RSS</sub>		4.6		pF

**Functional Tests** (In Demo Test Fixture, 50 ohm system) V<sub>DD</sub> = 28 Vdc, I<sub>DQ</sub> = 150mA, f = 150 MHz, Pin=2W, CW Signal Measurements.

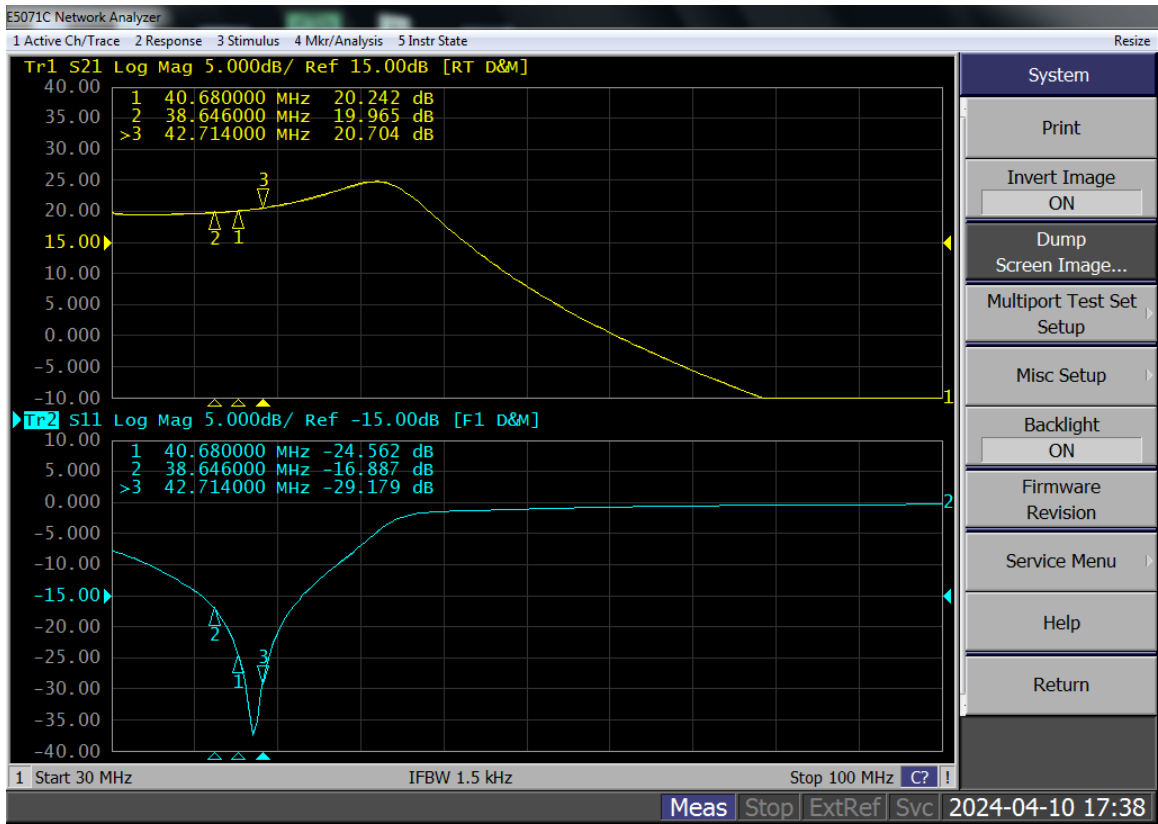
Power Gain	G <sub>p</sub>	—	20	—	dB
Drain Efficiency@Pout	η <sub>D</sub>	—	80	—	%
Output Power	P <sub>out</sub>	—	200	—	W
Input Return Loss	IRL	—	-7	—	dB

**Load Mismatch (In Innogration Test Fixture, 50 ohm system):** V<sub>DD</sub> = 28 Vdc, I<sub>DQ</sub> = 150 mA, f = 150 MHz

VSWR 20:1 at 200W pulse CW Output Power	No Device Degradation
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TYPICAL CHARACTERISTICS

Figure 1: Network analyzer output S11/221



Reference Circuit of Test Fixture Assembly Diagram (PCB file upon request)

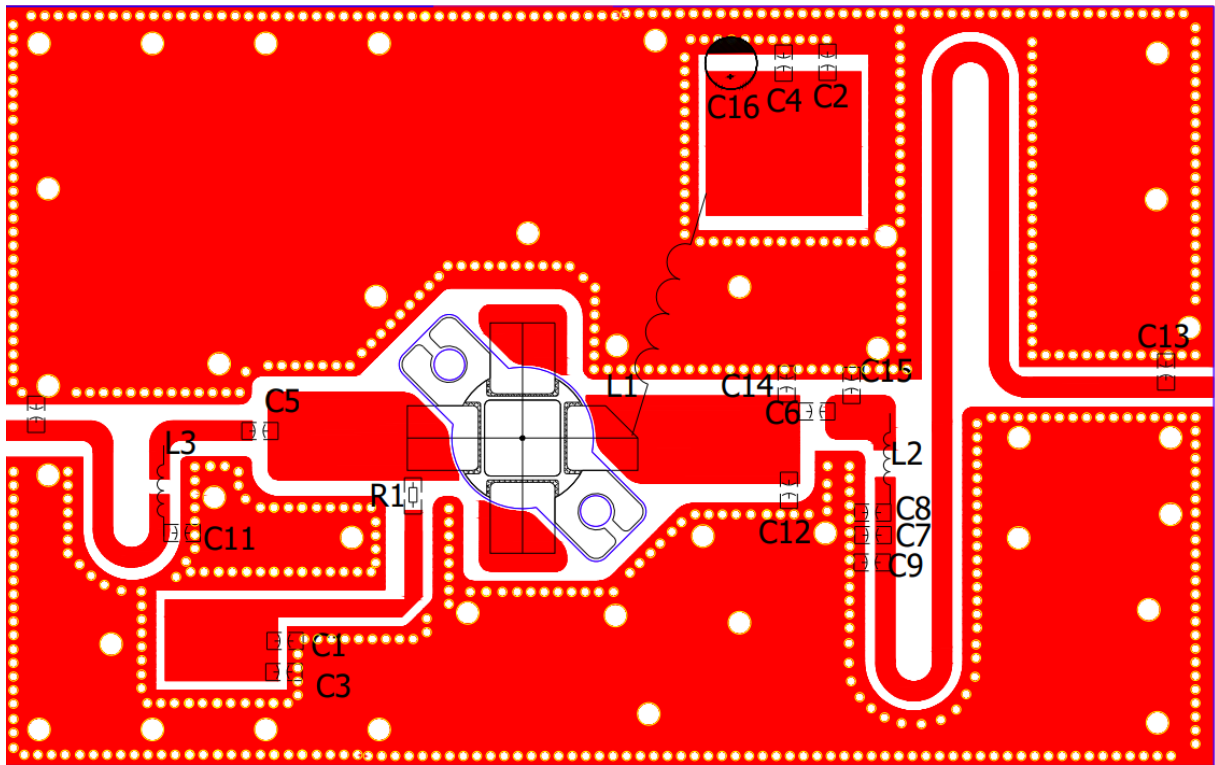
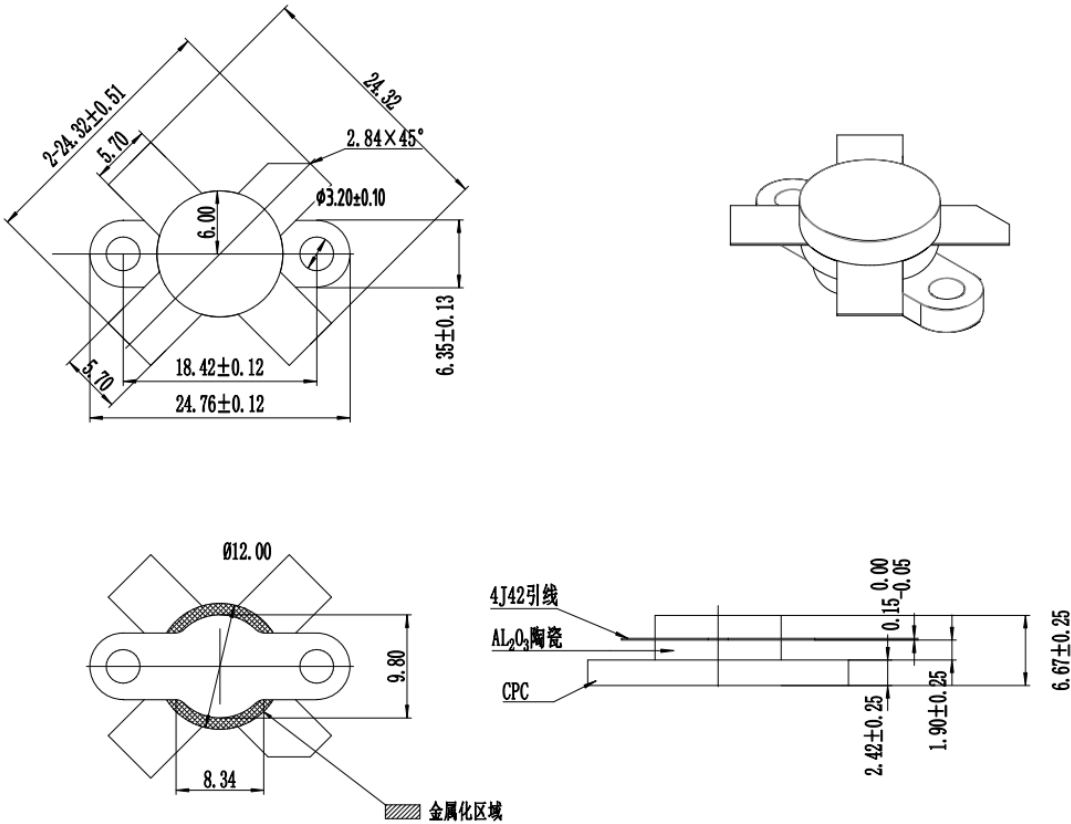


Table 1. Test Circuit Component Designations and Values (40.68MHz)

Component	Description	Suggestion
C1,C2	10uF	10uF/100V
C3~C6	10nF	10nF/100V
C7,C8	150pF	MQ101111
C9	39pF	MQ101111
C10	120pF	MQ101111
C11	47pF	MQ101111
C12	18pF	MQ101111
C13	12pF	MQ101111
C14	200pF	MQ101111
C15	470uF/63V	Electrolytic Capacitor
R1	10 $\Omega$	Chip Resistor
L1	1.5mm/5mm, 8 turns	
L2	1.5mm/5mm, 4 turns	
L3	1.5mm/5mm, 6 turns	
PCB	30Mil Rogers4350	

## Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads (1—Gate、2—Drain、3—Source)



### 技术要求:

1. 未注尺寸公差±0.15;
2. 全镀金: 外底面、内腔以及引线中心Ni:2.54-11.43 μm, 金2.54-4 μm;
3. 图示阴影部分为金属化区。
4. 单位:mm。

## Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/3/26	Rev 1.0	Preliminary datasheet
2025/1/13	Rev 1.1	Modify the PCB layout according to V4E package

Applicaion data based on TC-24-22

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