

S3K121K1V GaN TRANSISTOR

Document Number: S3K121K1V
Preliminary Datasheet V1.0

Gallium Nitride 50V, 1100W, RF Power Transistor

Description

The S3K121K1V is a 1100-watt, internally matched GaN HEMT, designed for pulsed amplifier applications with frequencies from 960MHz to 1200MHz.

There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

It is recommended to use this device only at pulse condition, and power rating will decrease according to longer pulse width and higher duty cycle

- Typical **pulse** Performance (On Innogration fixture with device soldered):

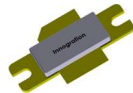
$V_{DD} = 50$ Volts, $I_{DQ} = 100$ mA, Pulse CW, Pulse width=20us, Duty cycle=10%.

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff (%)	P1dB Gain (dB)	P3dB (dBm)	P3dB (W)	P3dB Eff (%)
960	61.59	1442.7	60.9	17.3	62.11	1626.3	64.3
1010	61.15	1303.5	67.7	17.21	61.92	1557.2	72.7
1060	60.55	1136.0	70.1	17.14	61.24	1330.6	73.3
1110	60.18	1042.0	69.7	16.71	60.88	1224.6	72.7
1160	60.18	1043.2	67.9	17.6	60.77	1195.0	69.7
1215	60.26	1062.3	65.6	17.08	60.92	1236.3	67.4

S3K121K1VS



S3K121K1V



Applications and Features

- Suitable for broad band application in L band avionics
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

■ Turning the device ON

- 1) Set VGS to the pinch-off (VP) voltage, typically -5 V
- 2) Turn on VDS to nominal supply voltage (50 V)
- 3) Increase VGS until IDS current is attained
- 4) Apply RF input power to desired level

■ Turning the device OFF

- 1) Turn RF power off
- 2) Reduce VGS down to VP, typically -5 V
- 3) Reduce VDS down to 0 V
- 4) Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0	Vdc

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Operating Voltage	V_{DD}	0 to 55	Vdc
Maximum Forward Gate Current @ $T_C = 25^\circ\text{C}$	I_{gmax}	162	mA
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Case Operating Temperature	T_C	+150	$^\circ\text{C}$
Operating Junction Temperature	T_J	+225	$^\circ\text{C}$

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case, $P_{OUT}=1100\text{W}$ @1.1GHz 20us/10%, $T_{case}=85^\circ\text{C}$, 50 Vdc, $I_{DQ}=100\text{ mA}$	$R_{\theta JC}$	0.18	$^\circ\text{C/W}$

Table 3. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS}=-8\text{V}$; $I_{DS}=162\text{mA}$	V_{DSS}	---	200	---	V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 162\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS}=100\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$	---	-3.2	---	V

Functional Tests (In Innogration Test Fixture, 50 ohm system) : $V_{DD} = 50\text{Vdc}$, $I_{DQ} = 100\text{ mA}$, $f = 1100\text{MHz}$, Pulse CW, Pulse width=20us, Duty cycle=20%.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @ P_{-3dB}	G_P	---	16	---	dB
Drain Efficiency@ P_{SAT}	η_D	---	65	---	%
Saturated Power(P_{-3dB})	P_{SAT}	---	60.5	---	dBm
Input Return Loss	IRL	---	-5	---	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 50\text{ Vdc}$, $I_{DQ} = 100\text{ mA}$, $f = 1100\text{ MHz}$

VSWR 10:1 at 1100W pulse CW Output Power	No Device Degradation
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TYPICAL CHARACTERISTICS

Figure 2. Test Circuit Component Layout

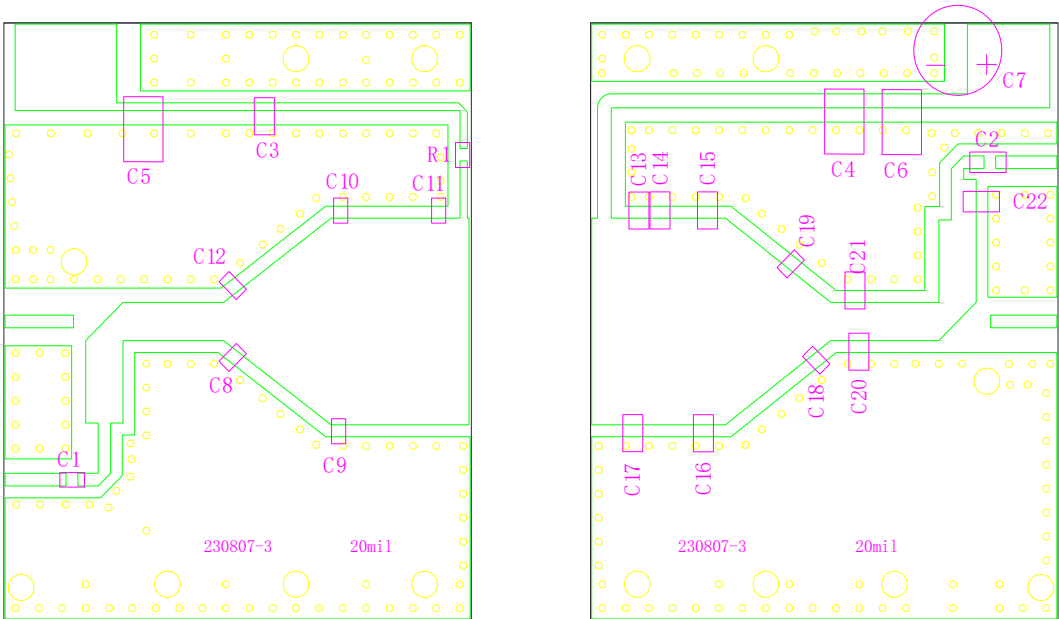


Table 4. Test Circuit Component Designations and Values

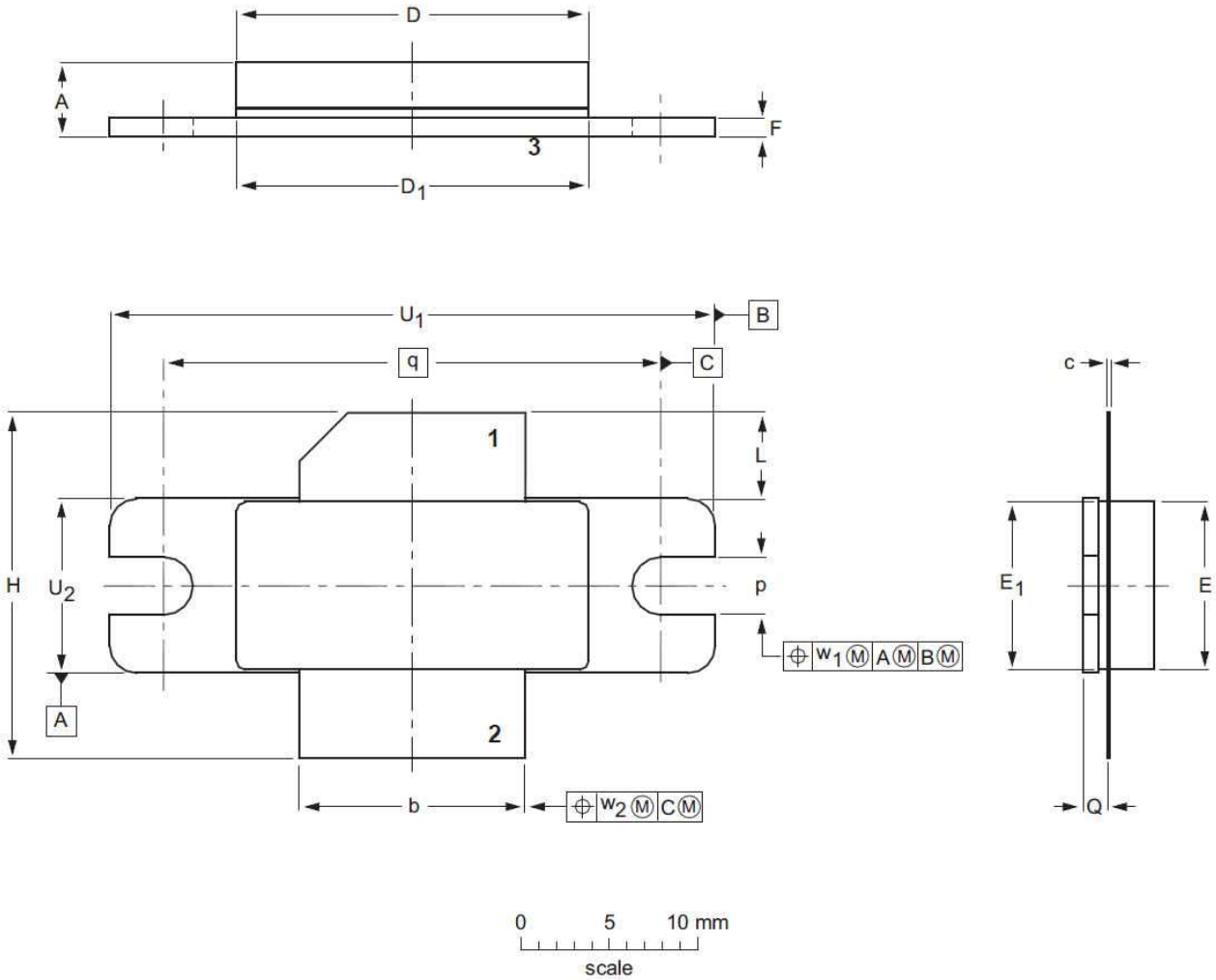
Designator	Comment	Footprint	Quantity
C1, C17	6.8 pF(High Q)	0805	2
C2, C4	47 pF (High Q)	1210	2
C3	47 pF (High Q)	0603/0805	1
C5, C6	10 uF/100V	1210	2
C7	1000 uF/63V		1
R1	10 Ω	0603	1
C8, C9, C10, C11, C13, C14, C15, C16	4.7pF (High Q)	0805	8
C12, C20	2.4 pF (High Q)	0805	2
C18, C19	2.0pF (High Q)	0805	2
C21, C22	1.0pF (High Q)	0805	3

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Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



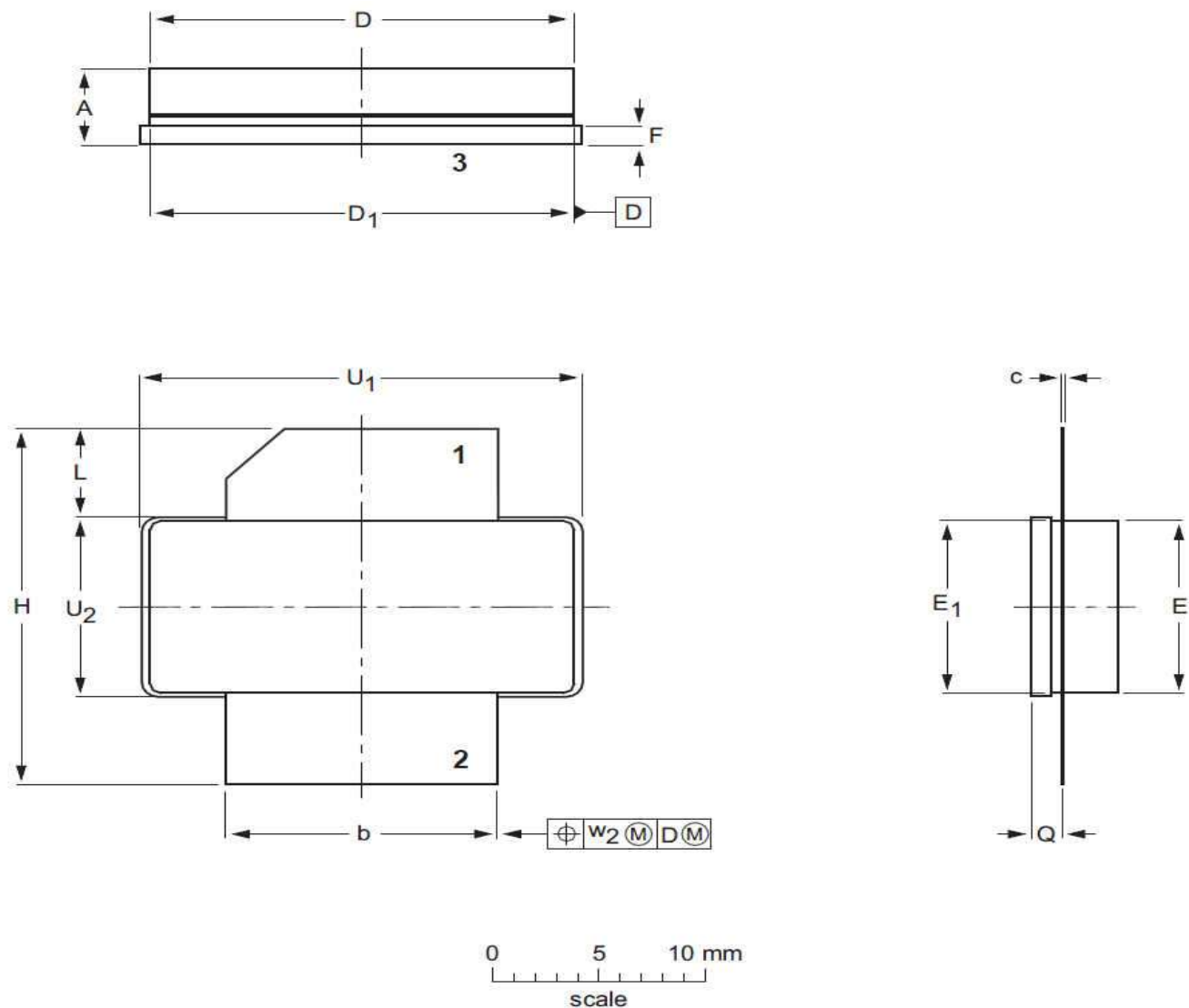
UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	p	Q	q	U ₁	U ₂	W ₁	W ₂
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	3.38	1.70	27.94	34.16	9.91	0.25	0.51
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	3.12	1.45		33.91	9.65		
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.133	0.067	1.100	1.345	0.390	0.01	0.02
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.123	0.057		1.335	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2E					03/12/2013

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Earless flanged ceramic package; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	Q	U ₁	U ₂	W ₂
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2024/5/17	Rev 1.0	Preliminary Datasheet,

Application data based on LSM-24-17

Notice

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