



## 0.2-4GHz, 25W, 2 stages 50V GaN Fully matched PA Module

### Description

The S2MAV0240-25 is a 25-watt ,2 stage integrated Power Amplifier Module, designed for broad band applications, with frequencies from 200MHz to 4GHz. The module is 50  $\Omega$  input/output matched and requires minimal external components.

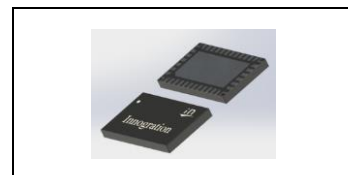
The module implements distributed power amplifier in form of multi chips, housed in cost effective plastic open cavity package, offers a much lower cost than traditional MMIC solutions.

It is recommended for pulse or back off condition, **NOT for CW operation.**

$V_{ds}=50V$ ,  $I_{DQ1}=20\text{ mA}$ ,  $I_{DQ2}=65\text{ mA}$ , Pulsed CW, 20us, 10%

| Parameter      | 0.2GHz | 1.0GHz | 2.0GHz | 3.0GHz | 4.0GHz | Units |
|----------------|--------|--------|--------|--------|--------|-------|
| Linear Gain    | 15.3   | 16.4   | 16.2   | 16.4   | 16.0   | dB    |
| Gain@Pin=31dBm | 13.5   | 14.3   | 14.3   | 14.1   | 13.3   | dB    |
| Pout@Pin=31dBm | 28.3   | 34.2   | 33.9   | 32.5   | 27.0   | W     |
| Eff@Pin=31dBm  | 40     | 41     | 36     | 35     | 34     | %     |

Recommended driver: SMAV0038-8



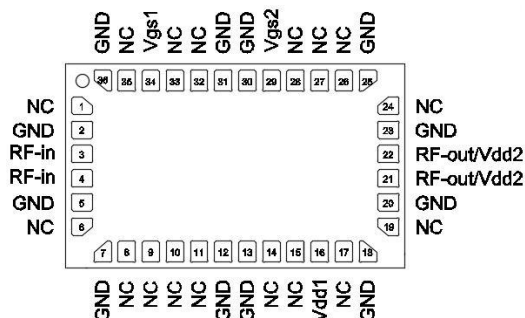
### Product Features

- Operating Frequency Range: 200MHz-4GHz
- Operating Drain Voltage: +50 V
- 50  $\Omega$  Input/Output
- Psat:  $\geq 25W$  (Pulsed only)
- Small signal gain:>15dB, Power gain:>13dB
- Minimum efficiency:30%
- 6x10 mm Surface Mount Package
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

### Applications

- Ultra Broadband Amplifiers
- L/S/C band pulsed power Amplifier
- Test Instrumentation
- EMC Amplifier Drivers
- 2-way Radios

### Pin Configuration and Description





| Pin No.                                          | Symbol     | Description                                                                                                                                                                                                |
|--------------------------------------------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 21,22                                            | RFout/Vdd2 | Transistor 1, Drain Bias2 & RF Output                                                                                                                                                                      |
| 3,4                                              | RFin       | Transistor 1, RF Input                                                                                                                                                                                     |
| 34                                               | Vgs2       | Transistor 1, Gate Bias1                                                                                                                                                                                   |
| 29                                               | Vgs2       | Transistor 1, Gate Bias2                                                                                                                                                                                   |
| 16                                               | Vdd1       | Transistor 1, Drain Bias1                                                                                                                                                                                  |
| Others                                           | NC         | No connection                                                                                                                                                                                              |
| 2,5,7,12, 13,18,20,23,25, 30, 31,36 Package Base | GND        | DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage. |

Table 1. Maximum Ratings

| Rating                         | Symbol    | Value       | Unit |
|--------------------------------|-----------|-------------|------|
| Drain--Source Voltage          | $V_{DS}$  | 200         | Vdc  |
| Gate--Source Voltage           | $V_{GS}$  | -10 to +2   | Vdc  |
| Operating Voltage              | $V_{DD}$  | +55         | Vdc  |
| Storage Temperature Range      | $T_{stg}$ | -65 to +150 | °C   |
| Case Operating Temperature     | $T_c$     | +150        | °C   |
| Operating Junction Temperature | $T_J$     | +225        | °C   |

Table 2. Thermal Characteristics

| Characteristic                                                             | Symbol          | Value | Unit |
|----------------------------------------------------------------------------|-----------------|-------|------|
| Thermal Resistance, Junction to Case<br>$T_c = 25^\circ\text{C}$ , DC test | $R_{\theta JC}$ | 2.9   | °C/W |

Table 3. Electrical Characteristics

| Parameter                    | Condition | Min | Typ | Max  | Unit |
|------------------------------|-----------|-----|-----|------|------|
| Frequency Range              |           | 200 |     | 4000 | MHz  |
| Power Gain @ Psat            |           | 13  |     |      | dB   |
| $P_{SAT}$                    |           |     | 25  |      | W    |
| Drain Efficiency @ $P_{SAT}$ |           | 30  |     |      | %    |

Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 50\text{ V}$ , Pulse Width=20 us, Duty cycle=10%Load Mismatch of per Section (On Test Fixture, 50 ohm system):  $V_{DD} = 50\text{ V}$ ,  $I_{DQ1+2} = 20+65\text{mA}$ ,  $f = 4\text{GHz}$ 

|                                         |                       |
|-----------------------------------------|-----------------------|
| VSWR 10:1 at Psat pulse CW Output Power | No Device Degradation |
|-----------------------------------------|-----------------------|

## Reference Circuit of Test Fixture Assembly Diagram

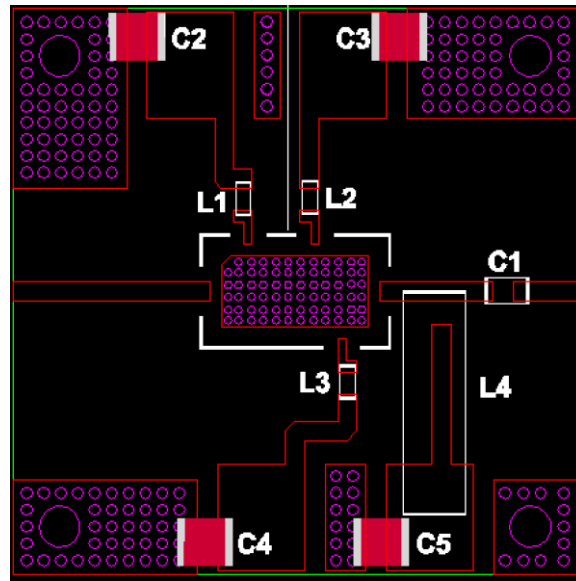


Figure 1. Test Circuit Component Layout

|             |                          | Part NO.            | Vendor    |
|-------------|--------------------------|---------------------|-----------|
| C1          | 50V 1uF Chip Capacitor   | GRM21BR71H105KA12L  | muRata    |
| C2,C3,C4,C5 | 10uF 100V Chip Capacitor | C5750X7S2A106M230KB | TDK       |
| L1, L2,L3   | 100 nH Capacitor(0603)   | LQW18CNR10K00D      | muRata    |
| L4          | 1.3uH 4.2A Inductor      | 4310LC-132KEC       | Coilcraft |
| PCB         | RO4350B,20mil,er=3.48    |                     |           |

## TYPICAL CHARACTERISTICS

Figure 2. Network analyzer output S11/S21 (Pin=0dBm)

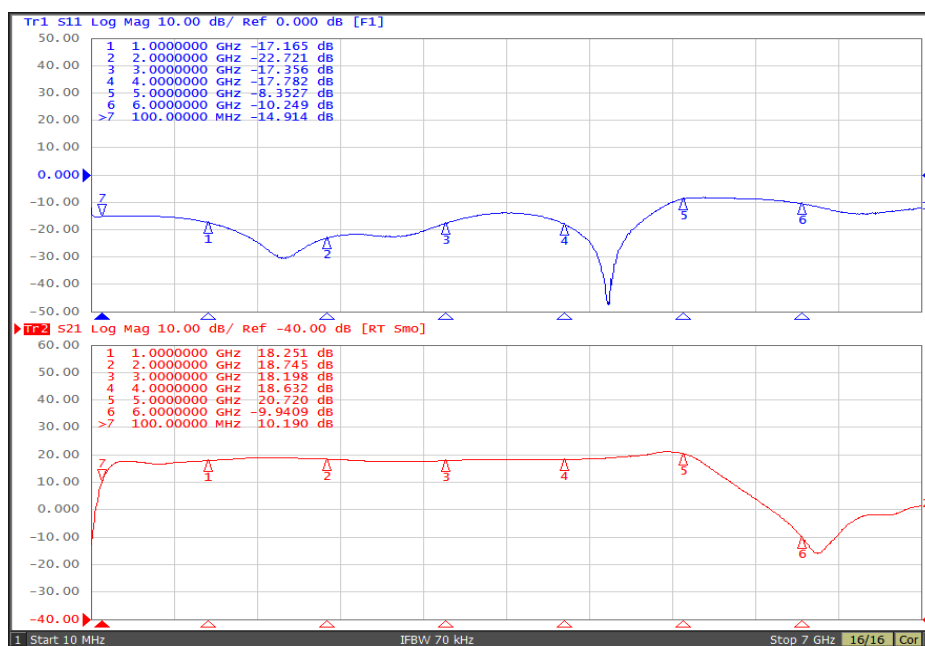
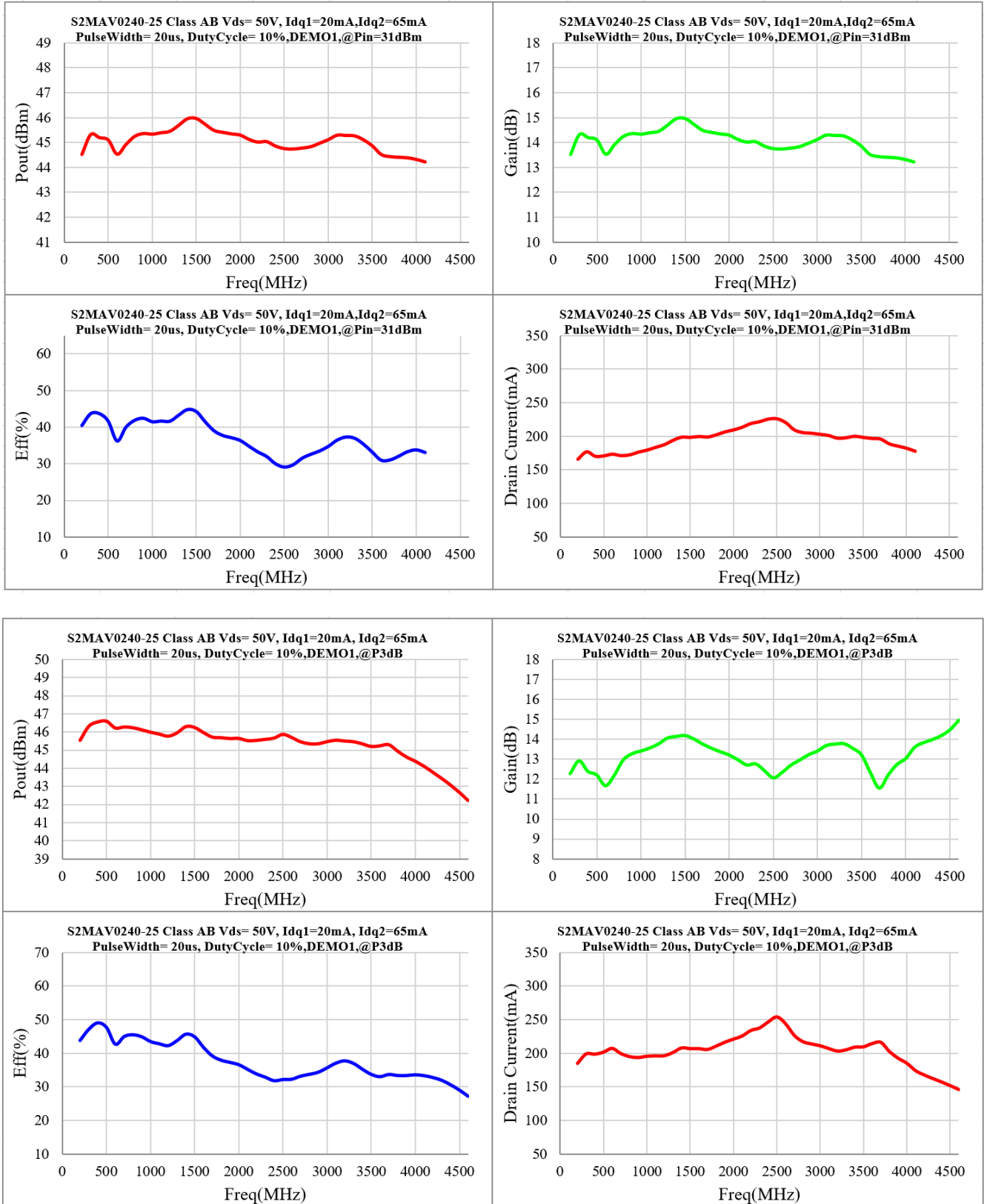


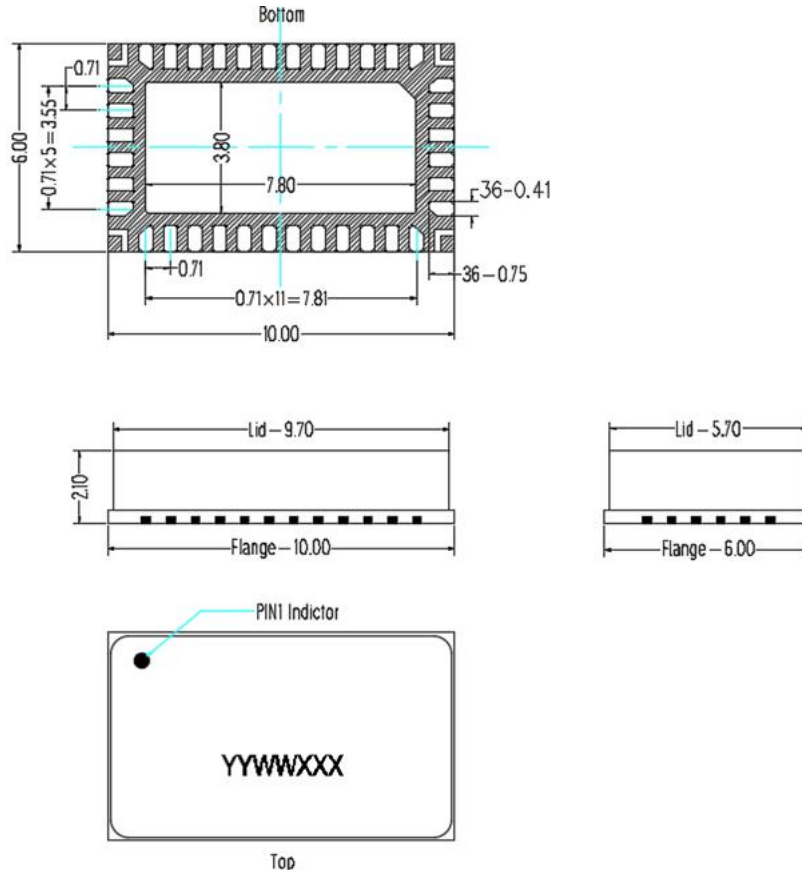


Figure 3. Psat, Power Gain and, efficiency vs. Frequency



## Package Dimensions

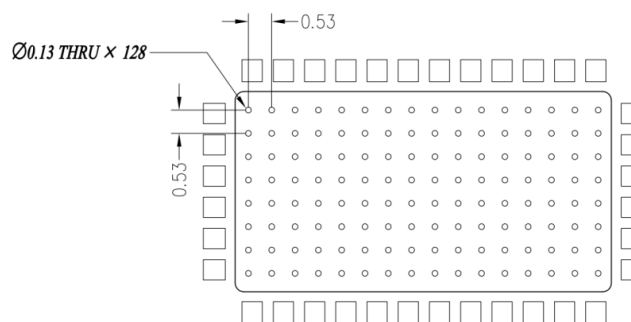
### 10\*6 Plastic Package



#### Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are  $\pm 0.2$ mm.

## Mounting Footprint Pattern



#### Notes:

1. All dimensions are in mm;
2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. ALL vias are PTH to ground.



## Revision history

Table 6. Document revision history

| Date      | Revision | Datasheet Status                                |
|-----------|----------|-------------------------------------------------|
| 2024/5/1  | V1.0     | Production datasheet                            |
| 2025/5/19 | V2.0     | Modify the PCB layout by split of Vgs1 and Vgs2 |
|           |          |                                                 |

Application data based on ZHH-24-07 /25-07(2\*2)

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