

NX4020RH GaN TRANSISTOR

Document Number: NX4020RH
Preliminary Datasheet V2.0

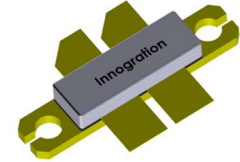
Gallium Nitride 28V 200W, RF Power Transistor

Description

The NX4020RH is a 200W 28V, GaN HEMT, designed for multiple applications with frequencies up to 3.2GHz.

There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.

NX4020RH



- Typical performance (on Innogrator wideband fixture with device soldered)

$V_{DD}=28V$ $I_{DQ}=80mA$, Pulsed CW 100us, 10%

Freq(MHz)	Pin(dBm)	Psat(dBm)	Psat(W)	Gain(dB)	Eff(%)
30	33	51.7	147.9	18.7	59.4
60	32.5	51.75	149.6	19.25	65.2
100	32.5	51.95	156.7	19.45	68.2
150	32.8	52.2	166.0	19.4	69.7
200	33.1	52.3	169.8	19.2	68.1
250	30.8	52.2	166.0	21.4	66.6
300	30.7	51.6	144.5	20.9	60.7
350	34.1	51.9	154.9	17.8	64.3
400	34.2	52.1	162.2	17.9	64.4
450	34.2	51.8	151.4	17.6	60.7
500	34.1	51.8	151.4	17.7	56.9
550	32.4	51.8	151.4	19.4	61.4
600	32.5	52.5	177.8	20	61.1
650	33.4	52.6	182.0	19.2	61.9
678	34.5	52.2	166.0	17.7	61.1

Applications and Features

- Suitable for wireless communication infrastructure, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage (28V)
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings (Not simultaneous, TC = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	150	Vdc

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Gate--Source Voltage	V_{GS}	-10,+2	Vdc
Operating Voltage	V_{DD}	40	Vdc
Maximum Forward Gate Current	I_{gmax}	49	mA
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature(See note 1)	T_j	+200	°C
Total Device Power Dissipation (Derated above 25°C, see note 2)	P_{diss}	205	W

1. Continuous operation at maximum junction temperature will affect MTTF
2. Bias Conditions should also satisfy the following expression: $P_{diss} < (T_j - T_c) / R_{JC}$ and $T_c = T_{case}$

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c = 85^\circ\text{C}$, $T_j = 200^\circ\text{C}$, DC Power Dissipation(See note 1)	$R_{\theta JC-DC}$	0.9	C/W

$R_{\theta JC-DC}$ is tested at only DC condition, it is related to the highest thermal resistor value among all test conditions. It might be differently lower in different RF operation conditions like CW signal ,pulsed RF signal etc.

Table 3. Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 49\text{mA}$	V_{DSS}	150			V
Gate Threshold Voltage	$V_{DS} = 28\text{V}$, $I_D = 49\text{mA}$	$V_{GS(th)}$		-2.7		V
Gate Quiescent Voltage	$V_{DS} = 28\text{V}$, $I_{DS} = 200\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-2.45		V

Functional Tests (In Innogration narrow band Test Fixture, 50 ohm system) : $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1400\text{ mA}$, $f = 1000\text{ MHz}$, CW

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @ P_{sat}	G_p		19		dB
Drain Efficiency @ P_{sat}	Eff		65		%
Saturated Power	P_{sat}		200		W
Input Return Loss	IRL		-7		dB
Mismatch stress at all phases (Device no damage)	VSWR		10:1		Ψ

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Figure 1: Network analyzer output, S11 and S21

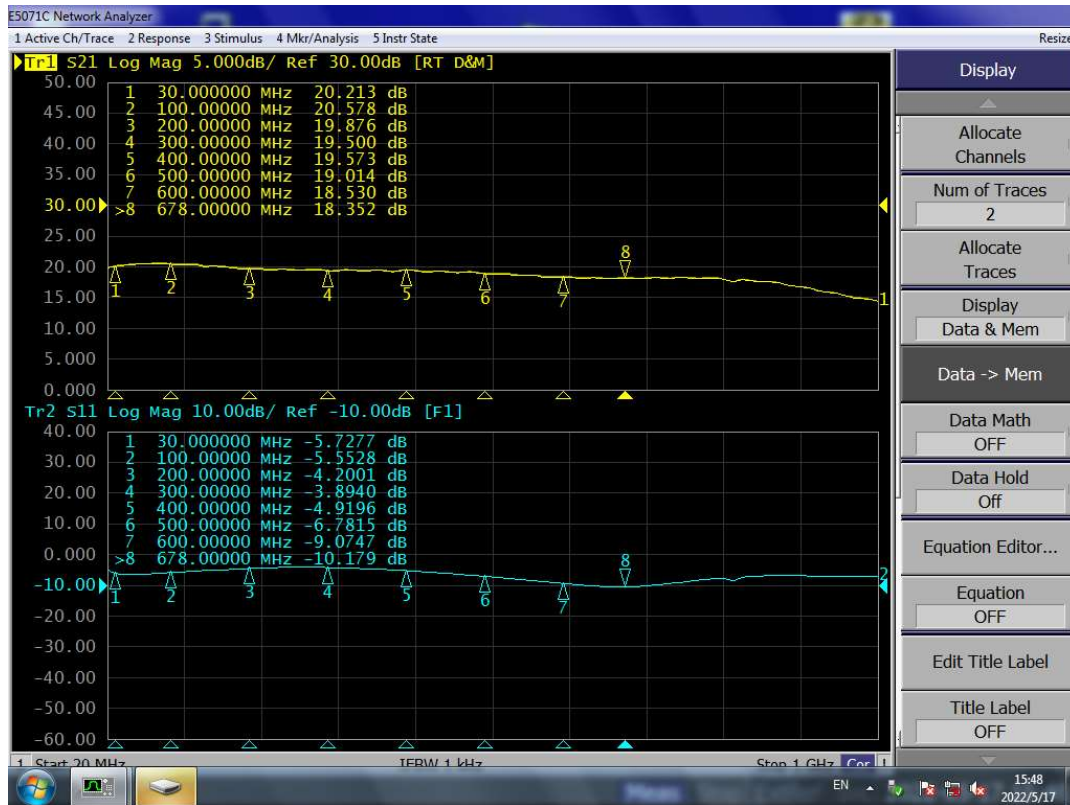


Table 4: IMD3 Vs Frequency at Pout=46dBm

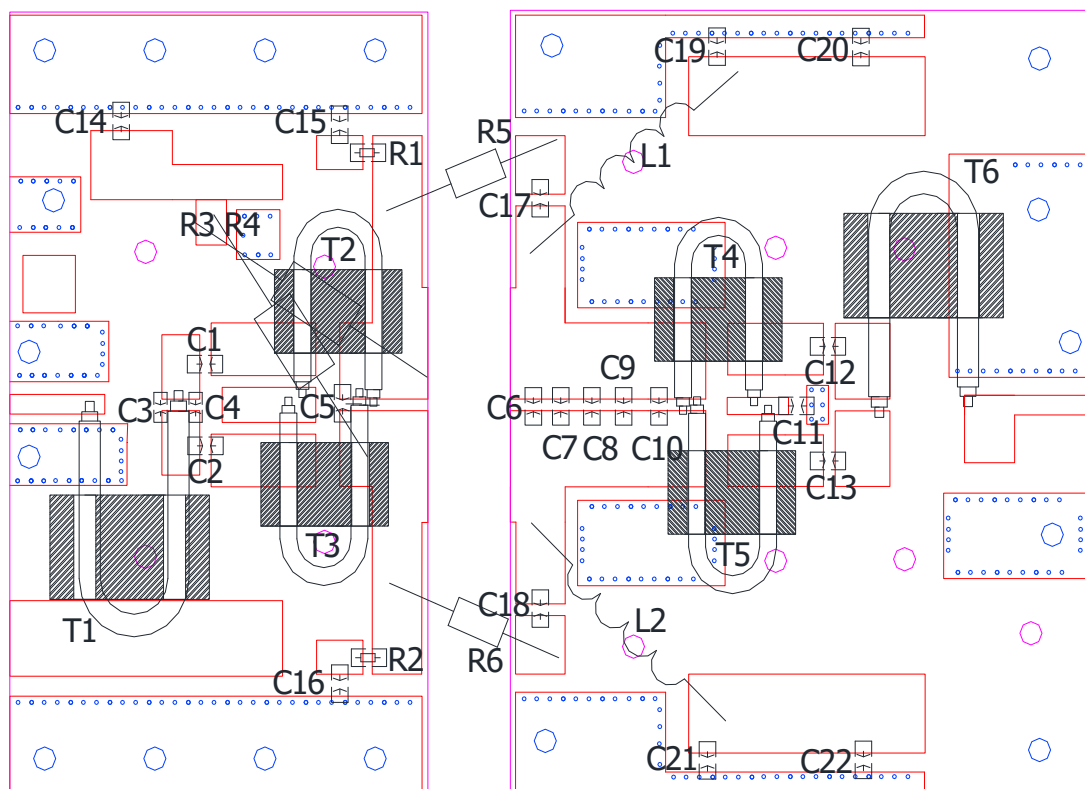
VDS=28V VGS=-2.61V IDQ=1700mA Signal mode: Two-tone spacing 2MHz

Freq(MHz)	Pin(dBm)	Pav(dBm)	Pav(W)	IDS(A)	Gain(dB)	Eff(%)	IMD3
30	22.7	46	39.8	4.39	23.3	32.4	-27
60	21.6	46	39.8	4.06	24.4	35.0	-28
100	22.4	46	39.8	3.98	23.6	35.7	-29
150	21.5	46	39.8	3.99	24.5	35.6	-29
200	22.2	46	39.8	4.16	23.8	34.2	-28
250	20.7	46	39.8	4.13	25.3	34.4	-26
300	22.1	46	39.8	3.92	23.9	36.3	-27
350	24.6	46	39.8	3.82	21.4	37.2	-29
400	24.6	46	39.8	3.89	21.4	36.6	-28
450	25.1	46	39.8	3.92	20.9	36.3	-30
500	24.4	46	39.8	4	21.6	35.5	-31
550	23.5	46	39.8	4.05	22.5	35.1	-31
600	23.5	46	39.8	4.3	22.5	33.1	-32
650	24.2	46	39.8	4.26	21.8	33.4	-30
678	25	46	39.8	4.11	21	34.6	-31

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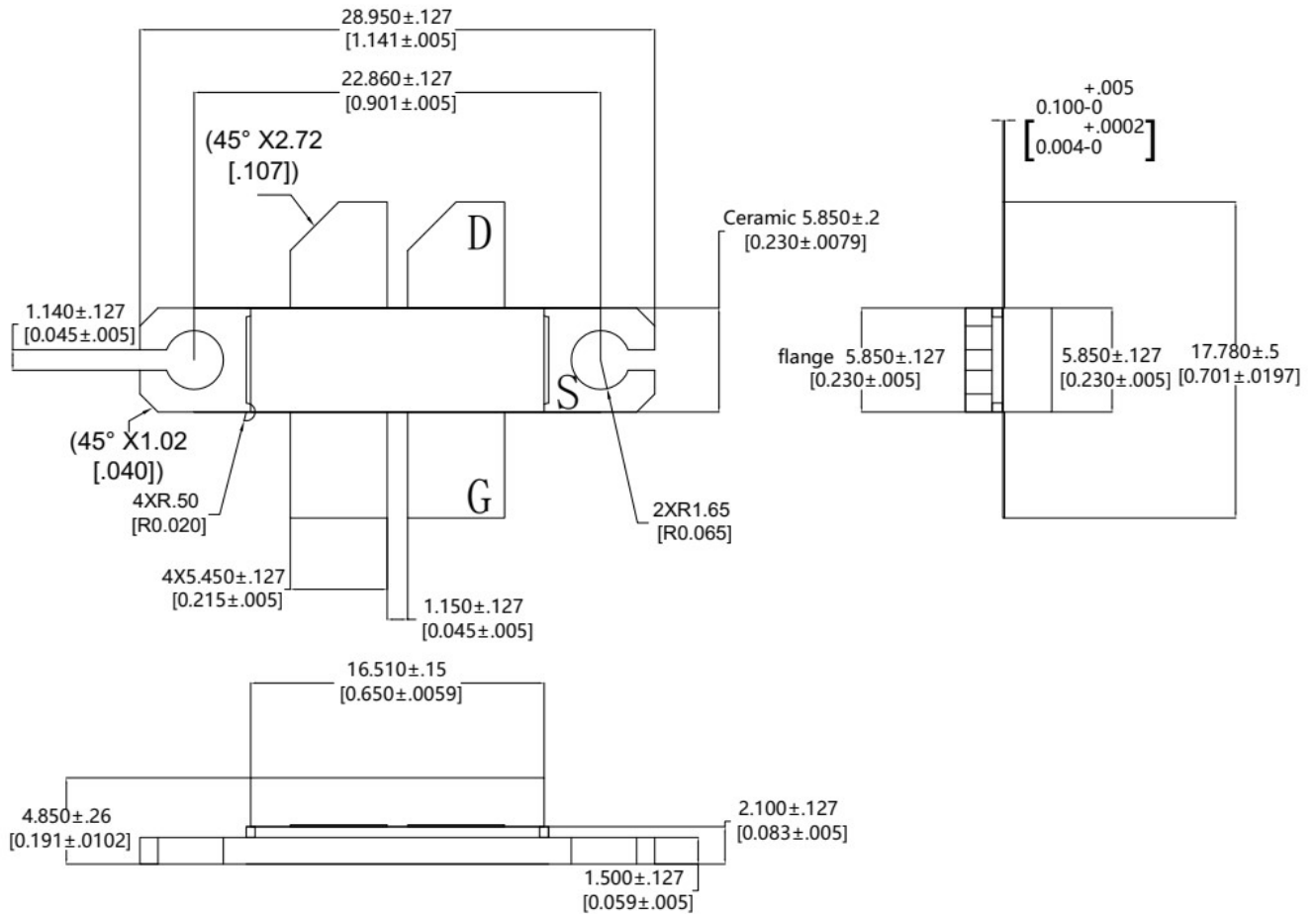
Figure 2: Picture of application board 30-678MHz class AB



Component	Description	Suggested Type
C1,C2,C12,C13,C17,C18	10nF	1812
C3,C4	05pF	MQ200805C0G2E0R5CNDB
C5	4.7pF	MQ101111M7G2H4R7NMB
C6	1pF	MQ101111M7G2H1R0NMB
C7	3.3pF	MQ101111M7G2H3R3NMB
C8	2pF	MQ101111M7G2H2R0NMB
C9	5.6pF	MQ101111M7G2H5R6NMB
C10	3pF	MQ101111M7G2H3R0NMB
C19,C21	470pF	ATC100B
C11,C14,C15,C16,C20,C22	10uF	10uF/50V
R1,R2	82Ω	0805
R3,R4	300Ω	3W/300Ω
R5,R6	300Ω	
T1,T6	50Ω,62mm	SF-086-50,BN-61-202
T2,T3,T4,T5	17Ω,62mm	SFF-17-1.5,BN-61-202
L1,L2	80nH	Manual made

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-LB					05/21/2021

Figure 1. Package Outline PKG-LB(LBB)

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Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2022/5/18	V1.0	Preliminary datasheet creation
2024/6/12	V2.0	Combine NX4020H and NX4020RH and state 3.2GHz supportable

Application data based on ZL-22-09

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