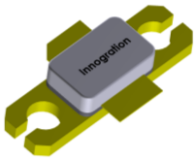
MU1513G LDMOS TRANSISTOR

Document Number: MU1513G
Preliminary Datasheet V1.1

40W, 12.5V High Power RF LDMOS FETs

MU1513G



Description

The MU1513G is a 40-watt P1dB (50W P3dB) high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 0.5 GHz.

•Typical 520MHz Performance (On Innogration fixture with device soldered):

V_{ds}= 12.5V, V_{gs}=2.49V,I_{dq}=120mA					
Test signal	**P-1(dBm)**	**P-1Gain(dB)**	**P-3(dBm)**	**P-3(W)**	**EFF (%)**
CW	**46.17**	**24.9**	**47.21**	**52.6**	**70.4**

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+28	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.58	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit

DC Characteristics

Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$	65	70		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 μA)	$V_{GS}(th)$	——	1.98	——	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.5	——	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V)	Rds(on)		110		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{ISS}		116		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{OSS}		50		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{RSS}		2		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 12.5 Vdc, I_{DQ} = 100 mA, f = 500 MHz, Pused CW Signal Measurements.

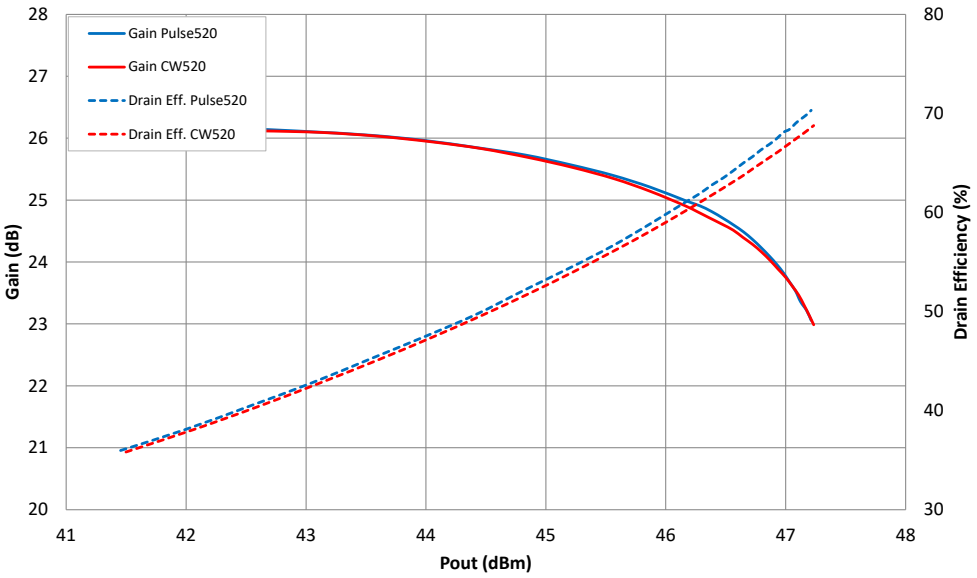
Power Gain	G_P	——	24	——	dB
Drain Efficiency@P1dB	η_D	——	65	——	%
1 dB Compression Point	P_{-1dB}	——	40	——	W

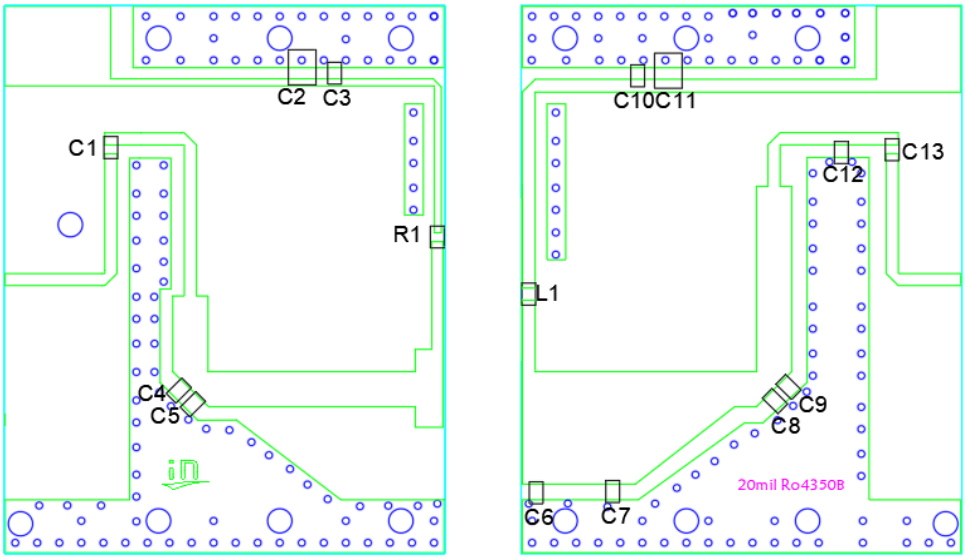
Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 12.5 Vdc, I_{DQ} = 100 mA, f = 500 MHz

VSWR 10:1 at 40W Pulsed CW Output Power	No Device Degradation

Figure 1： Network analyzer Output S11/S21

Figure 2: Power gain, efficiency as function of Pout

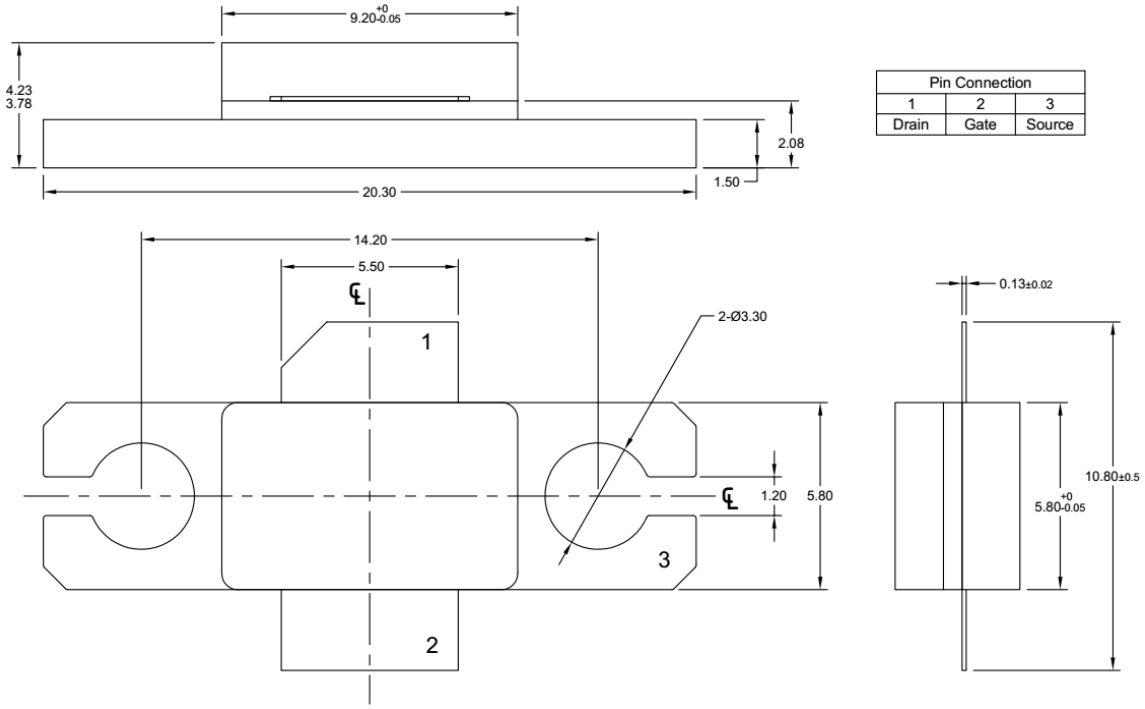




Component	Value	Description
C1,C3,C10,C13	220pF	MQ300805C
C2,C11	10uF	TDK1206
C4,C7	22pF	ATC600S
C5	5.1pF	ATC600S
C6	10pF	ATC600S
C8	20pF	ATC600S
C9	15pF	ATC600S
C12	1.8pF	ATC600S
R1	10Ω	--
L1	32nH	--

Package Outline

Flanged ceramic package; 2 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-GXB					10/10/2017

Figure 1. Package Outline PKG-G2E

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2024/6/5	Rev 1.0	Preliminary Datasheet Creation
2025/6/13	Rev 1.1	Update the performance summary on 1st page after recalibration

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