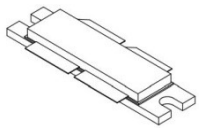
MQ0580X LDMOS TRANSISTOR

Document Number: MQ0580X
Preliminary Datasheet V1.0

600W, 28V High Power RF LDMOS FETs

MQ0580X



Description

The MQ0580X is a 600-watt capable, high ruggedness, high performance, unmatched push pull LDMOS FET,for commercial and industrial applications with frequencies HF to 100MHz. It can be used for both CW and pulse application or any other modulation signal.

It is featured for high power low thermal resistor, suitable for ISM applications, as well as FM radio, HF communication and mobile radio applications.

- Typical Performance at 28V (On Innogration 2-30MHz wideband fixture with device soldered):

MQ0580X Vgs=2.72V Vds=28V Idq=140mA CW						
Freq (MHz)	Psat (dBm)	Psat (W)	IDS (A)	Pin (dBm)	Gain (dB)	Eff(%)
2	56.03	400.9	18.84	37.50	18.53	75.99
4	56.11	408.3	19.00	37.05	19.06	76.75
6	56.34	430.5	20.05	37.00	19.34	76.69
10	56.76	474.2	21.55	36.30	20.46	78.59
15	57.29	535.8	23.81	36.15	21.14	80.37
20	57.54	567.5	25.62	36.10	21.44	79.12
25	57.59	574.1	26.68	35.85	21.74	76.85
30	57.55	568.9	27.27	35.80	21.75	74.50

24V data upon request

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI dri
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- RF generator at 2/13.56/27.12/40MHz etc

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.15	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$	95			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 800 μA)	$V_{GS}(th)$	——	2.2	——	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 2000 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3	——	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{ISS}		360		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{OSS}		160		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{RSS}		9		pF

2-30MHz

Reference Circuit of Test Fixture Assembly Diagram

(Layout file upon request, 30mil RO4350)

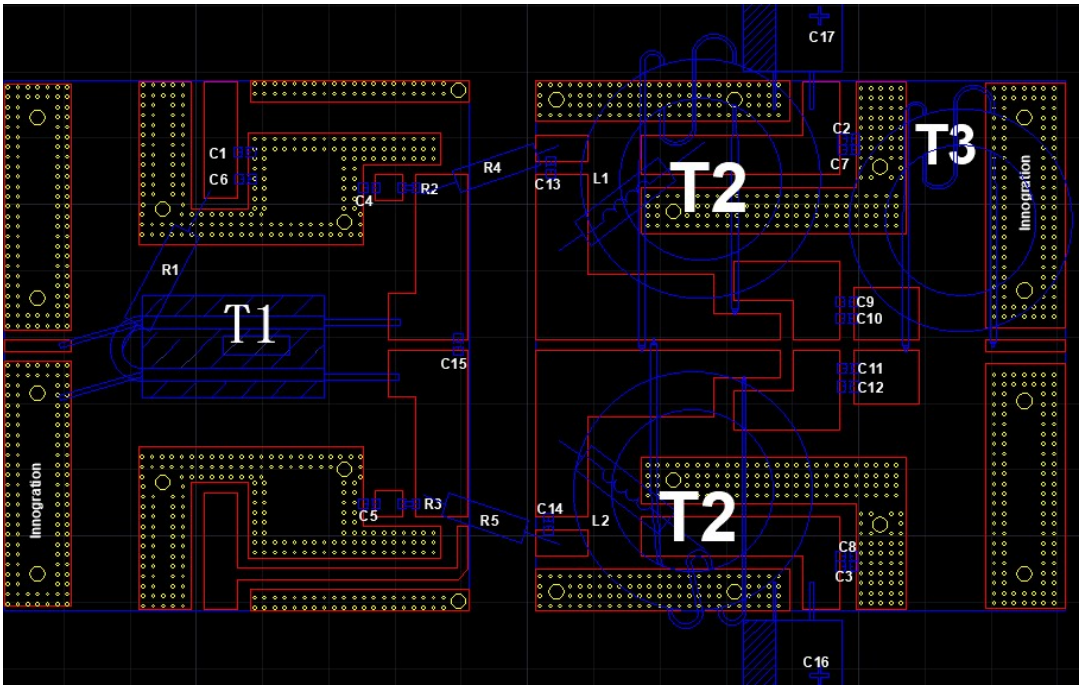
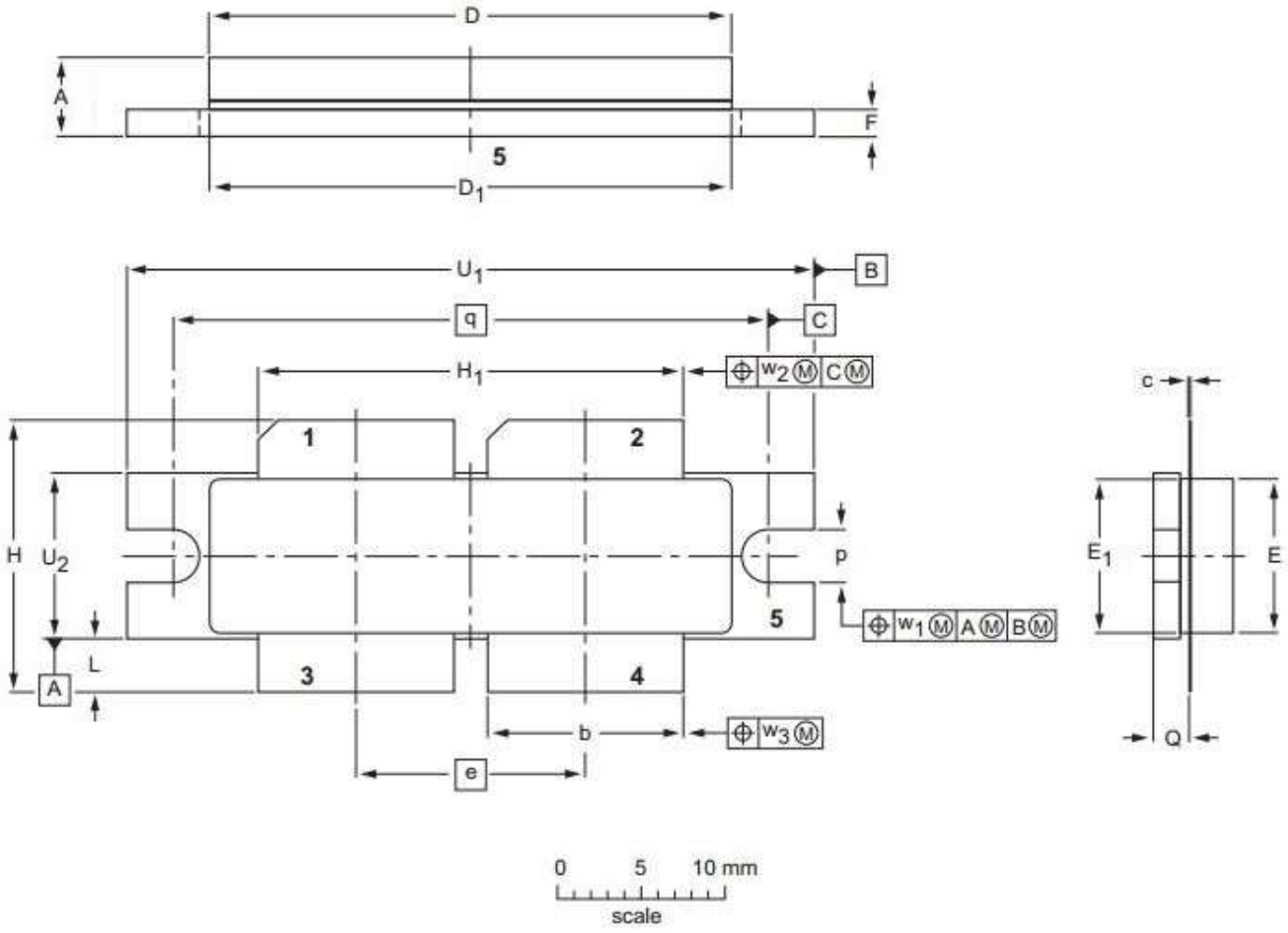


Table 5. Test Circuit Component Designations and Values

Component	Description	Suggestion
C1~C5	10uF/100V-1210	Ceramic multilayer capacitor
C6~C14	10nF/100V-1812	Ceramic multilayer capacitor
C15	180pF	BEIJING YUANLU HONGYUAN ELECTRONIC TECHNOLOGY CO., LTD.MQ301111
C16,C17	4700uF/63V	Electrolytic Capacitor
R1	330Ω-3W	Color ring resistance
R2,R3	33Ω-2512	Chip Resistor
R4，R5	100Ω-6W	Color ring resistance
L1,L2	1.2mm wire，11turns；FB-43-6251	DIY
T1	4：1 BN-43-3312	BN-43-3312
T2	12.5 ohm，550mm	SFF-12.5-1.5 , FT-140-43
T3	35 ohm，450mm	SFF-35-3 , FT-140-43
PCB	30Mil Rogers4350	

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	W_1	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2024/7/4	Rev 1.0	Preliminary Datasheet

Application data based on TC-24-41

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