MA1509 LDMOS TRANSISTOR

Document Number: MA1509
Preliminary Datasheet V1.0

90W, 28V High Power RF LDMOS FETs

MA1509

Description

The MA1509 is a 90-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies HF to 1.5 GHz. It can be used in Class AB/B and Class C for all typical modulation formats.

•Typical Performance (On Innogration fixture with device soldered):

MA1509 Vds=28V Vgs=3.02V Idq=200mA CW								
Freq(MHz)	**Pout(dBm)**	**Pout(W)**	**IDS(A)**	**Pin(dBm)**	**Gain(dB)**	**Eff(%)**	**2nd(dBc)**	**3rd(dBc)**
30	50.45	110.92	6.79	30.6	19.85	58.34	-20.4	-10.4
50	50.58	114.29	6.81	31.4	19.18	59.94	-24.1	-10.0
70	50.82	120.78	6.65	31.2	19.62	64.87	-27.5	-9.1
90	50.71	117.76	6.27	31.6	19.11	67.08	-29.9	-7.9
108	50.86	121.90	6.25	31.3	19.56	69.66	-31.3	-7.7

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+40	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$	95			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 150 μA)	$V_{GS}(th)$	——	2.17	——	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D =500 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.3	——	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{ISS}		54		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{OSS}		18		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{RSS}		1.2		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 500 mA, f = 1000 MHz, CW Signal Measurements.

Power Gain	G_p		18		dB
Drain Efficiency@P1dB	η_D		60		%
1 dB Compression Point	P_{-1dB}		90		W
Input Return Loss	IRL		-7		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 500 mA, f = 1000 MHz

VSWR 20:1 at 90W pulse CW Output Power	No Device Degradation

Figure 2. Test Circuit Component Layout

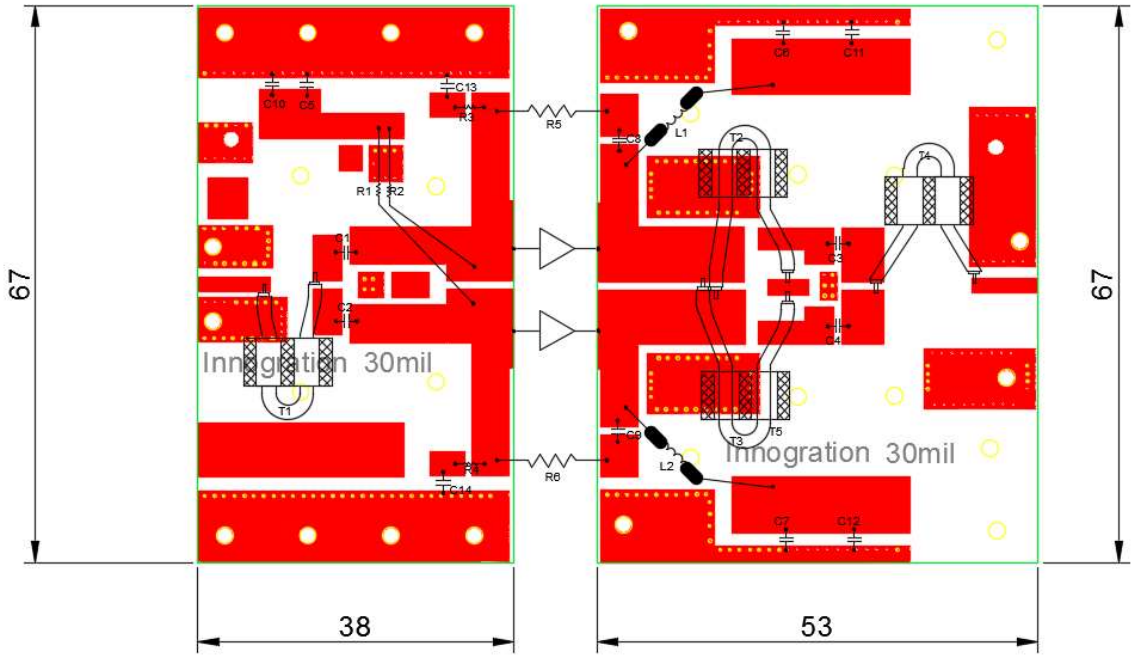
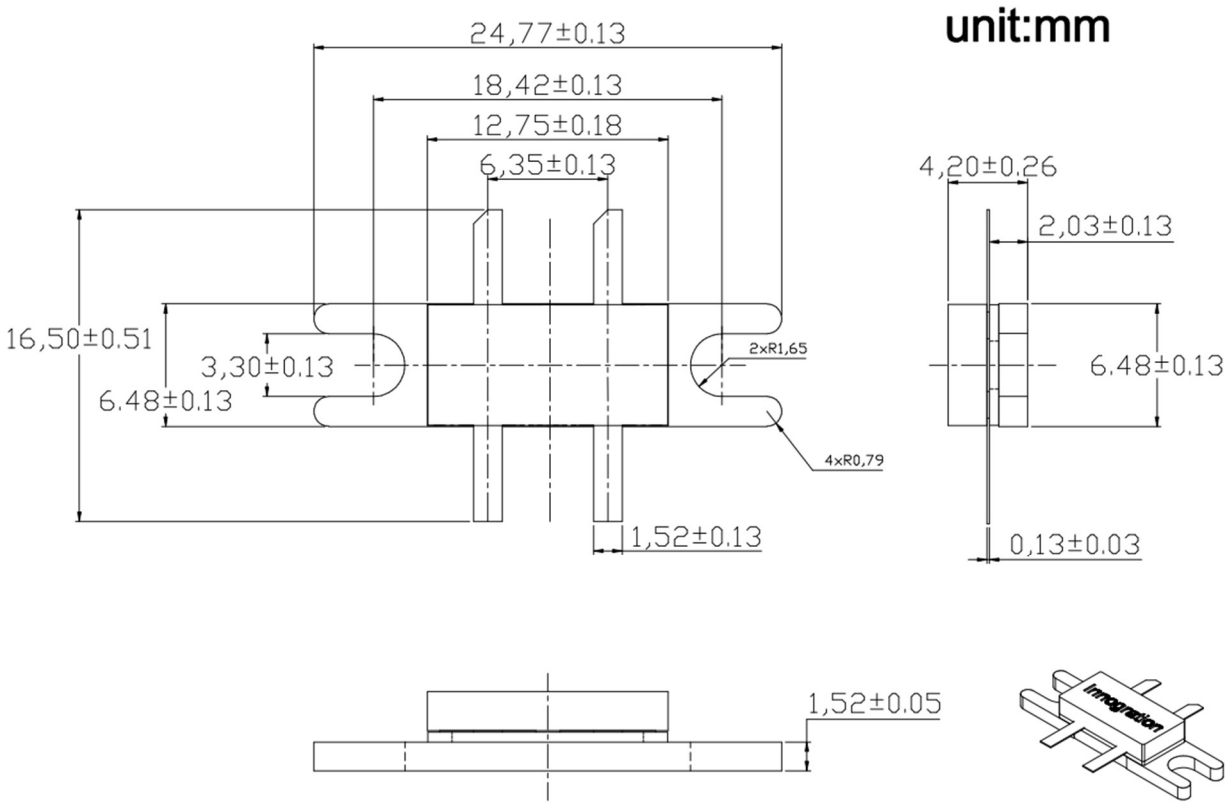


Table 5. Test Circuit Component Designations and Values

Part	description	Model
C1~C4	560pF	MQ101111
C5~C9	1000pF	MQ101111
C10~C12	10uF	Ceramic multilayer capacitor
C13，C14	10nF	Ceramic multilayer capacitor
R1,R2	220 Ω	Pulg-in Resistor
R3,R4	300 Ω	Chip Resistor
R5,R6	500 Ω	Pulg-in Resistor
L1,L2	d=1.5mm，D=4.2mm，13 turns	DIY
T1,T4	50ohm 70mm	BN-61-202 RFSFBU-086-50
T2,T3	25ohm 70mm	BN-61-202 SFF-25-1.5

Package Outline



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2024/3/28	**Rev 1.0**	**Preliminary Datasheet**

Application data based on HL-24-12

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