



GaN 50V,700W, RF Power Transistor

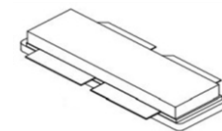
SQ1071RVPS

Description

The SQ1071RVPS is a push pull 700W capable, internally matched GaN HEMT, ideal for multiple applications up to 1GHz. It is optimized thermally to support higher duty cycle or longer pulse up to CW application.

In typical wideband application from 500 to 900MHz and 100-600MHz it can deliver >450W CW across the full band.

There is no guarantee of performance when this part is used outside of stated frequencies.



- Typical CW performance at 500-900MHz applications, $V_{ds}=50V$, $I_{dq}=120mA$, $V_{gs}=-3.50V$

Freq (MHz)	Psat (dBm)	Psat (W)	Ids (A)	Pin (dBm)	Gain (dB)	Eff (%)	2 nd (dBc)	3 rd (dBc)
500	57.06	508.2	15.16	42.78	14.28	67.04	-22	-13
550	58.46	701.5	18.65	43.12	15.34	75.22	-28	-24
600	57.69	587.5	16.86	41.21	16.48	69.69	-24.5	-29.7
650	57.08	510.5	16.51	40.99	16.09	61.84	-23.4	-33.7
700	56.96	496.6	17.62	40.06	16.9	56.37	-26.7	-30.8
750	57.17	521.2	15.9	39.85	17.32	65.56	-31	-42
800	58.02	633.9	20	40.68	17.34	63.39	-36	-49
850	58.47	703.1	20.74	40.23	18.24	67.80	-28	-41
900	57.15	518.8	14.5	39.22	17.93	71.56	-37.4	-51.9

- Typical CW performance at 100-600MHz applications, $V_{ds}=50V$, $I_{dq}=120mA$, $V_{gs}=-3.50V$

Freq (MHz)	Psat (dBm)	Psat (W)	Ids (A)	Pin (dBm)	Gain (dB)	Eff (%)	2 nd (dBc)	3 rd (dBc)
100	57.32	539.5	16.08	35.87	21.45	67.10	-30.8	-10.5
150	58.06	639.7	20.03	37.16	20.9	63.88	-31.3	-9.3
200	58.45	699.8	20.78	36.37	22.08	67.36	-33.1	-10.3
250	57.83	606.7	19.28	37.46	20.37	62.94	-26.9	-9.5
300	57.54	567.5	18.88	37.66	19.88	60.12	-30	-35
350	58.2	660.7	19.95	36.44	21.76	66.23	-35	-25.4
400	58.21	662.2	19.38	35.94	22.27	68.34	-37.6	-27.2
450	57.57	571.5	17.34	36.83	20.74	65.91	-60	-19.5
500	57.57	571.5	17.15	36.59	20.98	66.64	-60	-18.4
550	57.58	572.8	18.17	36.97	20.61	63.05	-47	-28.4
600	57.11	514.0	16.97	37.72	19.39	60.58	-49.2	-30.3

Applications

- P band power amplifier
- UHF TV
- Public Safety Radio
- Data link power amplifier



Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch-off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	I_{gs}	86.6	mA
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_C = 25^\circ\text{C}$, at $P_{out} = 700\text{W}$ @900MHz	$R_{\theta JC}$	0.21	°C /W

Table 3. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 43.2\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 43.2\text{mA}$	$V_{GS(th)}$	-4	-	-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS} = 100\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.5		V

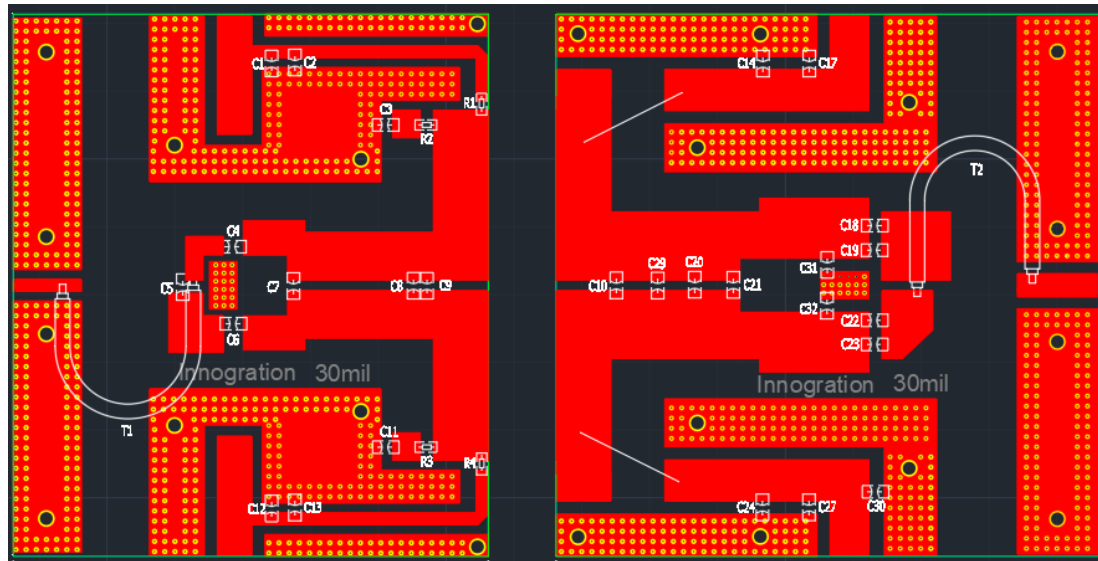
Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	900MHz, $P_{out} = 700\text{W}$ pulse CW All phase, No device damages	VSWR		5:1		



500-900MHz

Figure 1: Reference design circuit (PCB DWG file upon request,)

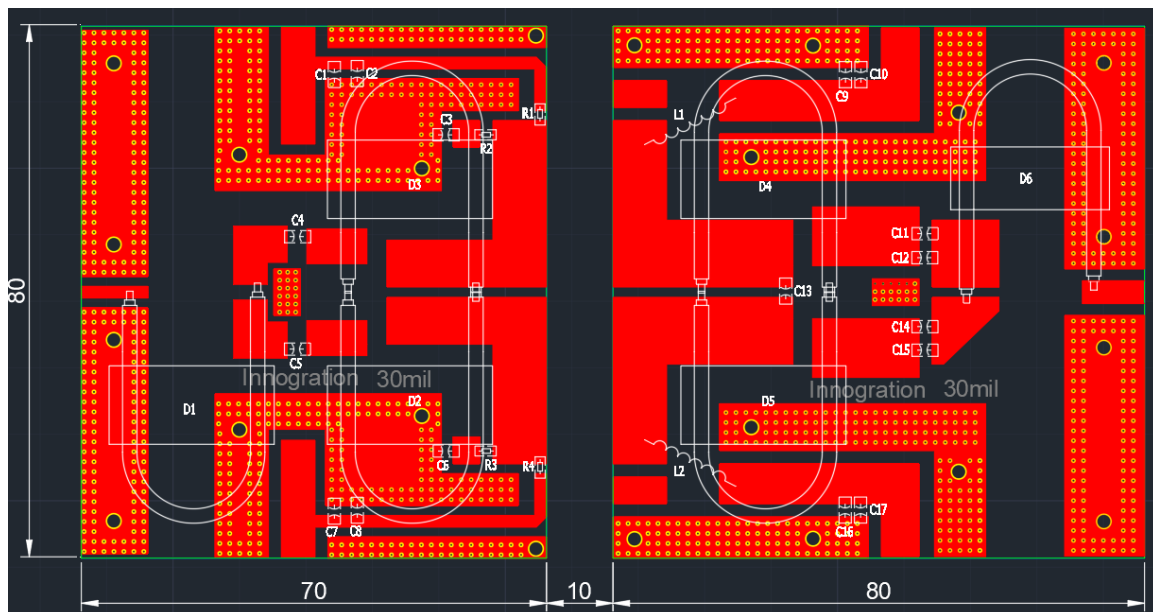


C1,C12,C17,C27	10uF	/
C2,C4,C6,C13	36pF/MQ301111	
C3,C11	1000pF/MQ301111	
C14,C24	120pF/MQ301111	
C18,C19,C22,C23	18pF/MQ301111	
C5,C10	1.5pF/MQ301111	
C7	1pF/MQ301111	
C8	3.6pF/MQ301111	
C9	10pF/MQ301111	
C10	10pF/MQ301111	
C20,C21,C31,C32	3pF/MQ301111	
C29	0.5pF/MQ301111	
C30	4700uF/63V	/
R1,R4	300Ω/1206	/
R2,R3	10Ω/1206	/
T1	50ohm,50mm	RFSFBU-086-50
T2	35ohm,70mm	SFF-35-3
PCB	30mil TC350	



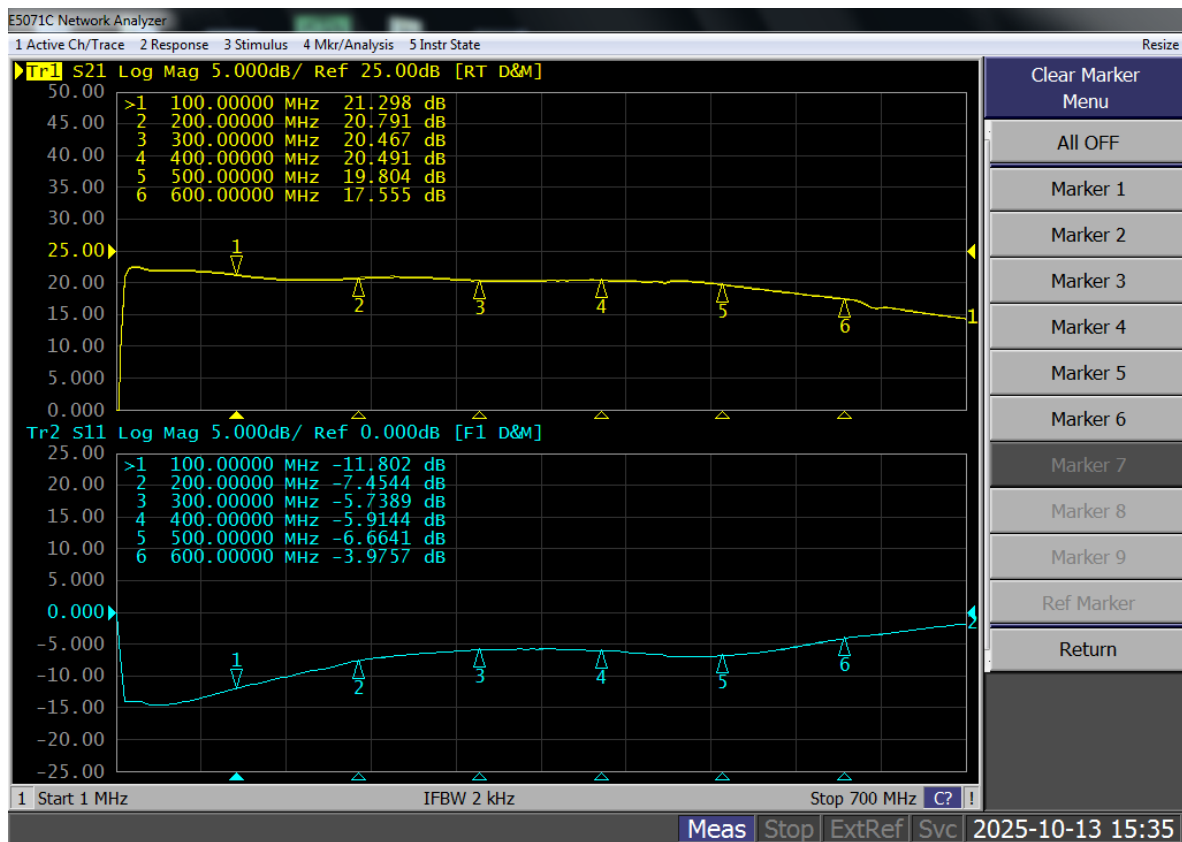
100-600MHz

Figure 3: Reference design circuit (PCB DWG file upon request,)





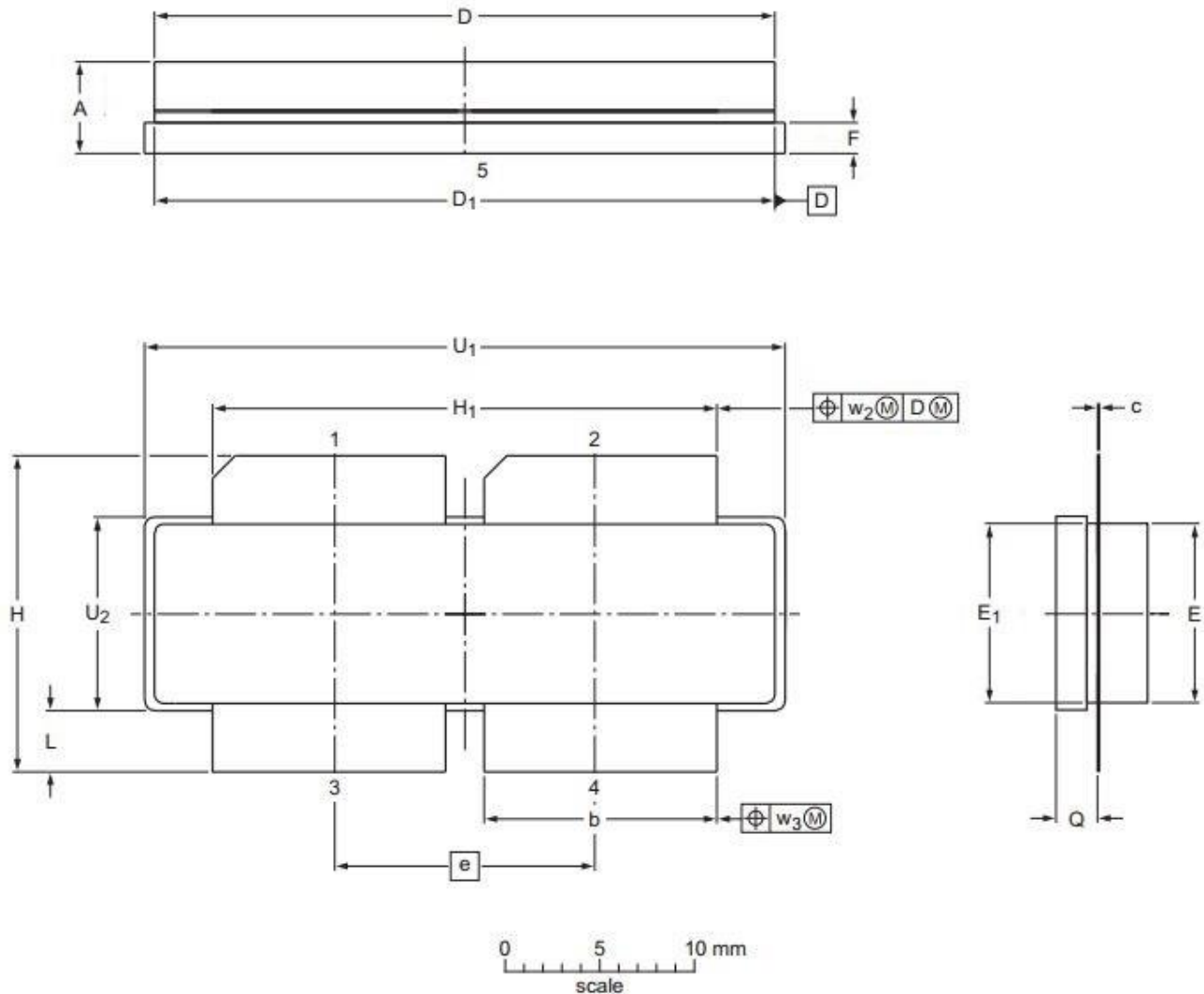
C1,C3,C6,C7,C10,C17	10uF	/
C2,C4,C5,C8,C9,C16	1000pF/MQ301111	
C11,C12,C14,C15	470pF/MQ301111	
C13	10pF/MQ301111	
R1,R4	300Ω/1206	/
R2,R3	10Ω/0805	/
D1	50ohm,70mm, BN-61-202	RFSFBU-086-50
D2,D3	16.7ohm,70mm, BN-61-202	SFF-16.7-1.5
D4,D5	16.7ohm,110mm,BN-61-002	SFF-16.7-3
D6	50ohm,100mm,BN-61-002	SFF-50-3





Package Outline

Earless flanged ceramic package; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₂	W ₂
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2025/10/11	V1.0	Preliminary Datasheet Creation based on V1 to replace SQ1070RVPS

Application data based on: SJJ-25-28/29

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