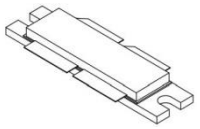
M2Q0571VPX LDMOS TRANSISTOR

Document Number: M2Q0571VPX
Preliminary Datasheet V1.0

700W, 50V High Power RF LDMOS FETs

M2Q0571VPX



Description

The M2Q0571VPX is a 700-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 700MHz. It can be used for both CW and pulse application.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.

It is the gain enhanced version of MQ0571VPX at higher frequency.

- Typical Performance (On Innogration 15-520MHz wideband fixture with device soldered):

V_{DD} = 50 Volts, I_{DQ} = 200 mA, CW,

Freq (MHz)	Pin (dBm)	Psat (dBm)	Psat (W)	IDS (A)	Gain (dB)	Eff (%)	2nd Harmonic(dBc)	3rd Harmonic(dBc)
15	37.3	57.16	520	14.5	19.9	72.0	-25.0	-10.3
20	37.0	57.42	552	15.1	20.4	73.1	-24.8	-10.4
50	37.1	57.76	597	17.1	20.7	70.0	-29.1	-12.8
100	38.9	57.32	540	18.7	18.5	57.7	-31.0	-10.0
150	38.4	56.62	459	18.8	18.2	48.9	-33.6	-10.2
200	38.9	57.04	506	19.6	18.1	51.6	-37.0	-10.0
250	38.5	57.32	540	20.0	18.8	54.0	-42.3	-18.8
300	37.8	57.12	515	19.3	19.3	53.4	-41.2	-23.3
350	37.8	56.97	498	18.3	19.2	54.4	-47.0	41.0
400	37.1	56.47	444	17.0	19.4	52.2	-49.0	-44.0
450	39.0	56.59	456	18.9	17.6	48.3	-46.6	-35.5
500	40.0	56.86	485	20.4	16.9	47.6	-60.0	-25.0
520	40.0	56.16	413	17.0	16.2	48.6	-57.5	-37.0

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- On chip RC network enable high stability and ruggedness
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	135	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 80°C, 700W CW, 50 Vdc, I_{DQ} = 200 mA	$R_{\theta JC}$	0.13	°C/W
Transient thermal impedance from junction to case Tj = 150° C; tp = 100 us; Duty cycle = 20 %	Zth	0.04	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

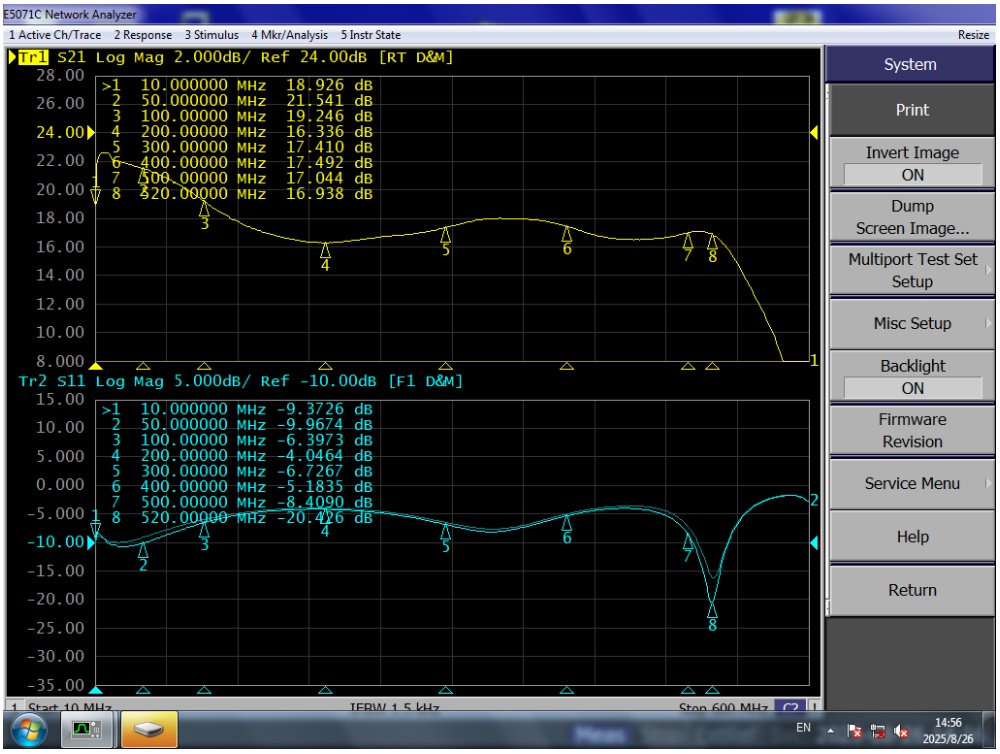
Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		135		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.68	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.0	——	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured	Rds(on)		180		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		280		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		80		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		1.5		pF

15-520MHz

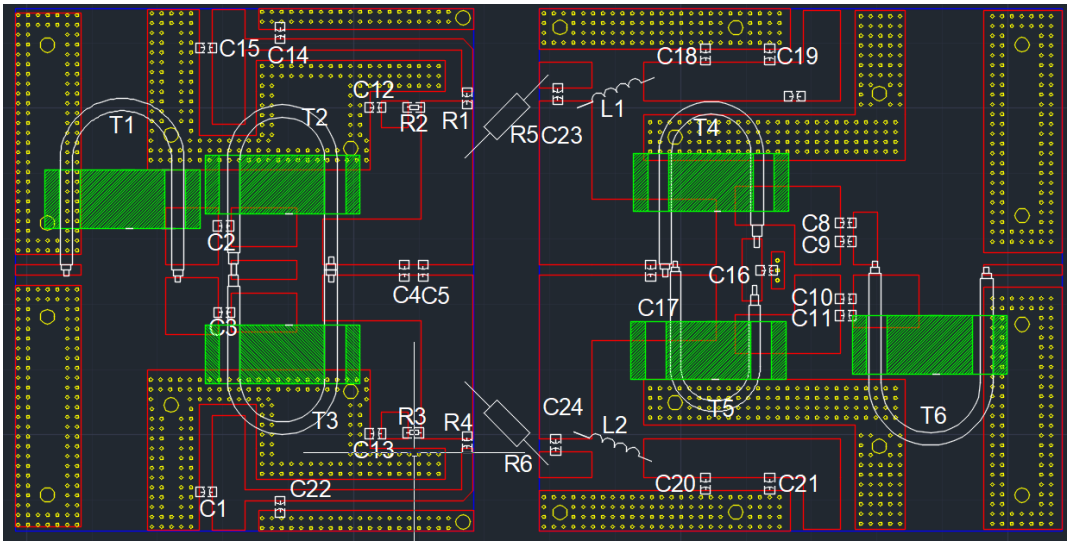
TYPICAL CHARACTERISTICS

Figure 1: Network analyzer output S11/S21 at 50V Idq=1000mA



Reference Circuit of Test Fixture Assembly Diagram

(Layout file upon request, 30mil RO4350)



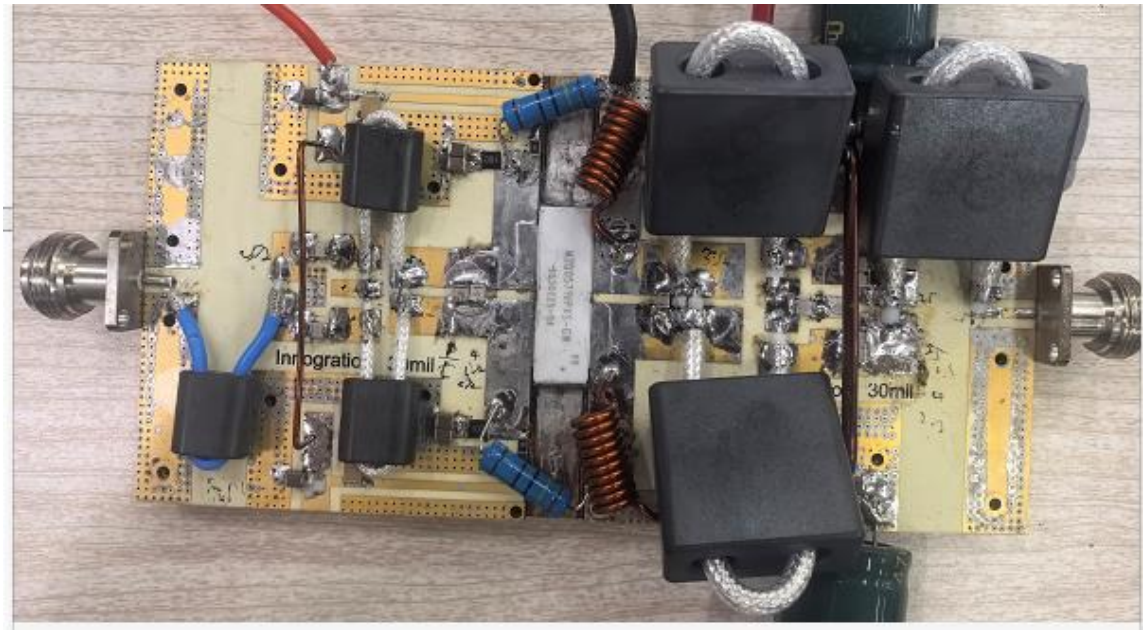
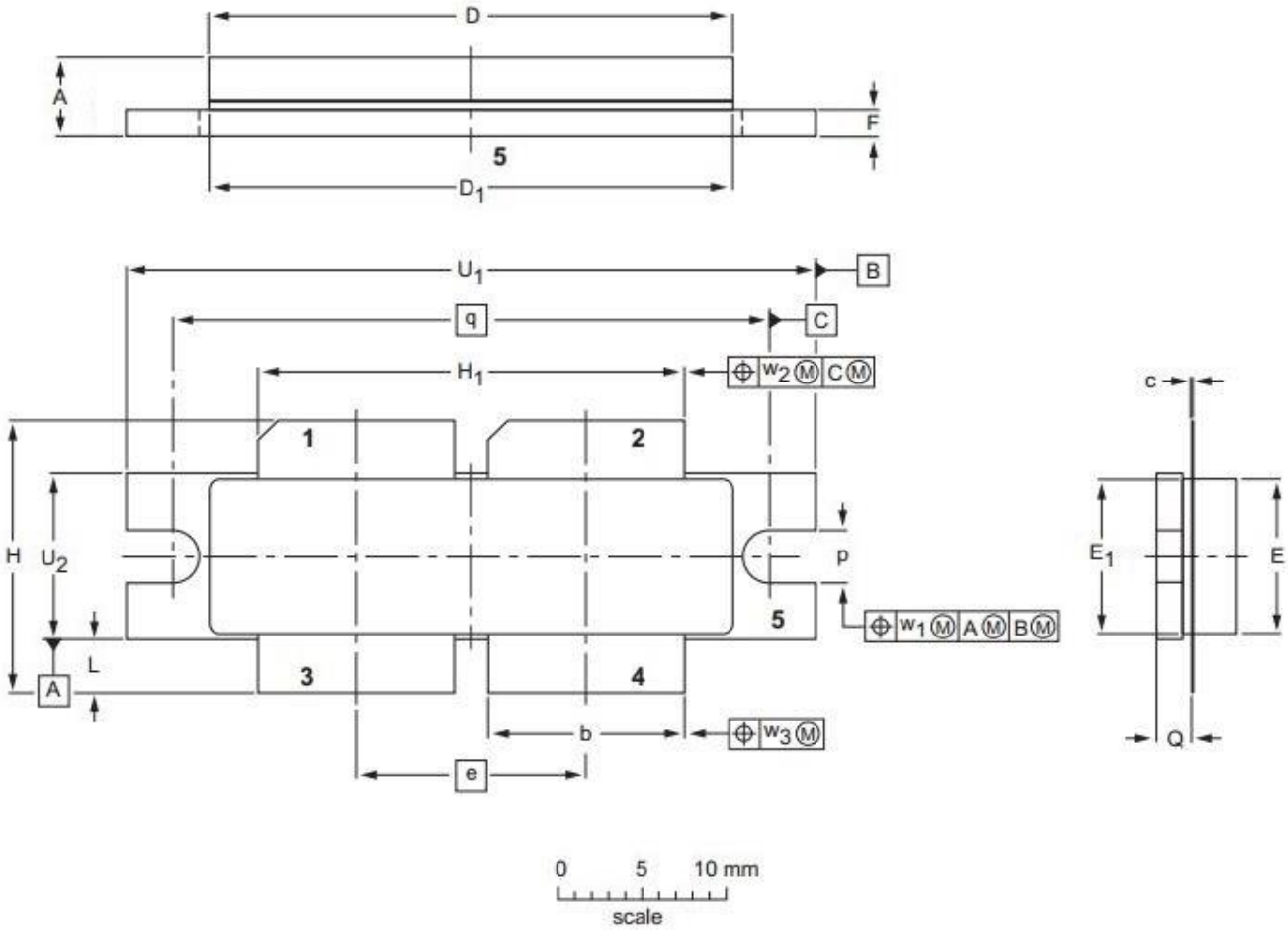


Table 5. Test Circuit Component Designations and Values

Component	Description	Suggestion
C2,C3,C8~C11	470pF/ MQ101111	
C1,C12,C13,C19,C21,C15	10uF /1210	//
C14,C22,C18,C20,C23,C24	10nF /1210	//
C4	10Pf/MQ301111	
C5	47Pf/MQ301111	
C16	680Pf/MQ101111	
C17	30Pf/MQ101111	
R1,R4	360Ω/1206	//
R2,R3	10Ω/1812	//
R5,R6	240Ω/1W	//
T1	50ohm,75mm	BN-61-202
T2,T3	12.5ohm,65mm	BN-61-202
T4,T5	25ohm,100mm	BN-61-002
T6	35ohm,100mm	BN-61-002
L1,L2	1.5 mm wire, 10Turns , 5mm inner diameter,	DIY

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	W_1	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/8/26	Rev 1.0	Preliminary Datasheet

Application data based on SYX-25-31

Disclaimers