



GaN 50V, 300W, 2-3G RF Power Transistor

Description

The STBV27W300BY2 is a single ended 300watt capable, broadband GaN HEMT, ideal for ISM and Telecom especially CW applications within full band of 2-3GHz.

In typical 2.3-2.7GHz, It can deliver >300W CW with higher effi

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical CW performance at 2.3--2.7GHz applications

$V_{DD} = 50$ Vdc, $V_{GS} = -4.5$ V, with device soldered, CW:

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff (%)	P1dB Gain (dB)	P3dB (dBm)	P3dB (W)	P3dB Eff (%)
2300	55.45	350.6	67.5	15.33	55.89	387.9	69.6
2400	55.29	338.5	68.7	16.05	55.85	384.5	71.0
2500	55.13	325.6	69.8	16.18	55.77	377.8	72.4
2600	54.69	294.5	65.6	15.72	55.4	346.7	68.1
2700	54.46	279.2	65.0	15.21	55.21	331.8	67.5

Recommended driver: STAV58025P2

Applications

- 2.45GHz RF Energy
- S band power amplifier
- N41 mobile broadband

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set V_{GS} to the pinch-off (V_P) voltage, typically -5 V
2. Turn on V_{DS} to nominal supply voltage
3. Increase V_{GS} until I_{DS} current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce V_{GS} down to V_P , typically -5 V
3. Reduce V_{DS} down to 0 V
4. Turn off V_{GS}

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	I_{GS}	43.2	mA
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_C = 25^\circ\text{C}$, at $P_d = 160$ W	$R_{\theta JC}$	0.78	°C /W

STBV27W300BY2

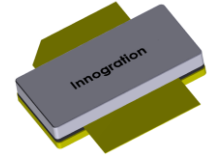




Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics (measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=43.2mA	V _{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 43.2mA	V _{GS(th)}	-4	-	-2	V
Gate Quiescent Voltage	VDS =50V, IDS=100mA, Measured in Functional Test	V _{GS(Q)}		-3.7		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.45GHz, Pout=300W pulse CW All phase, No device damages	VSWR		10:1		

TYPICAL CHARACTERISTICS

Figure 1: Efficiency and power gain as function of Pout (VDD = 50Vdc, Vgs=-4.5V, Pulse width=20us, duty cycle=20%)

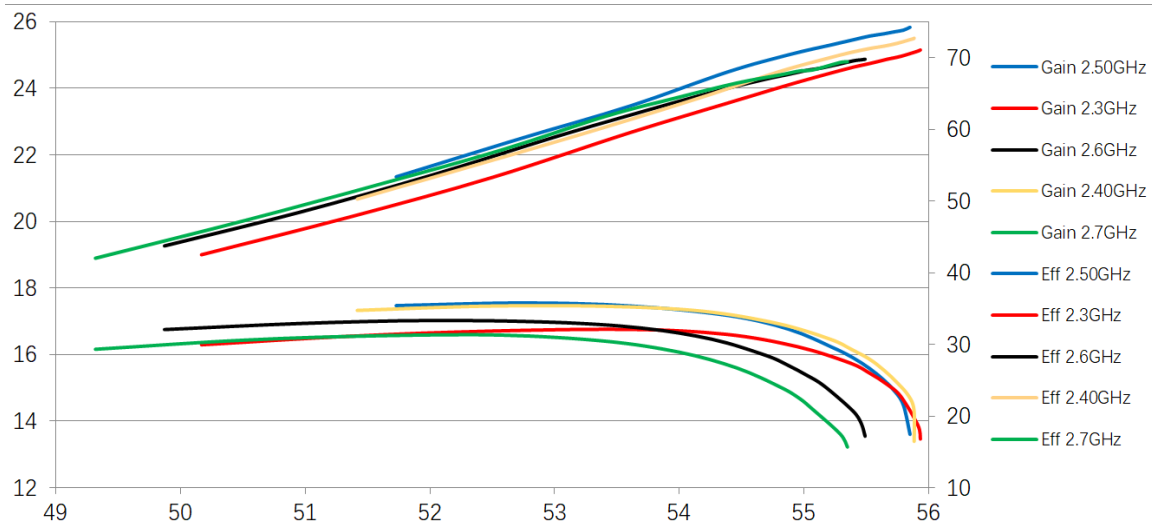
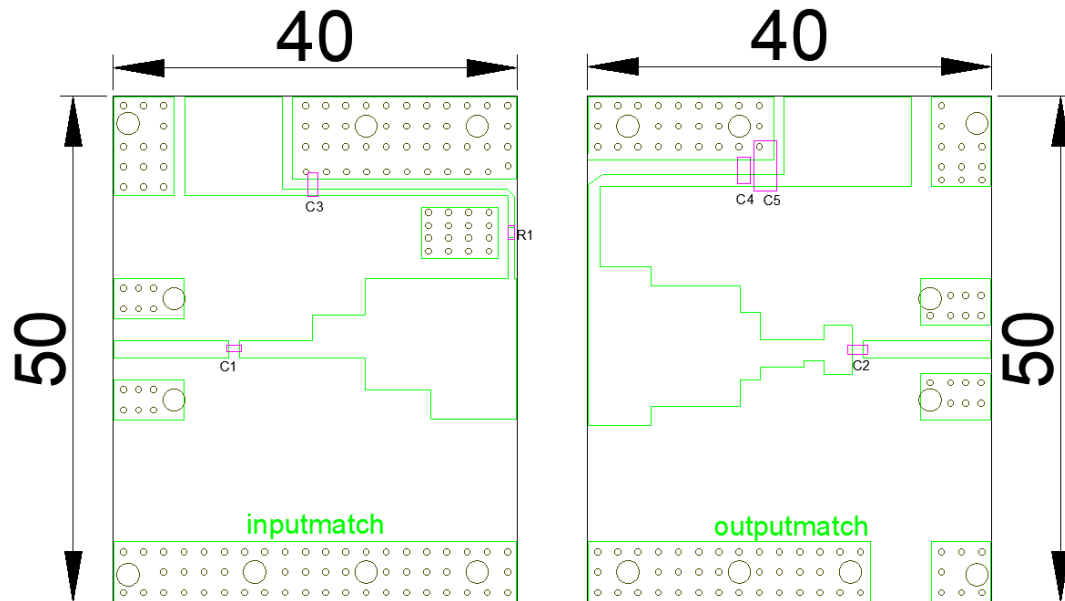




Figure 2: Reference design circuit (PCB DWG file upon request,)

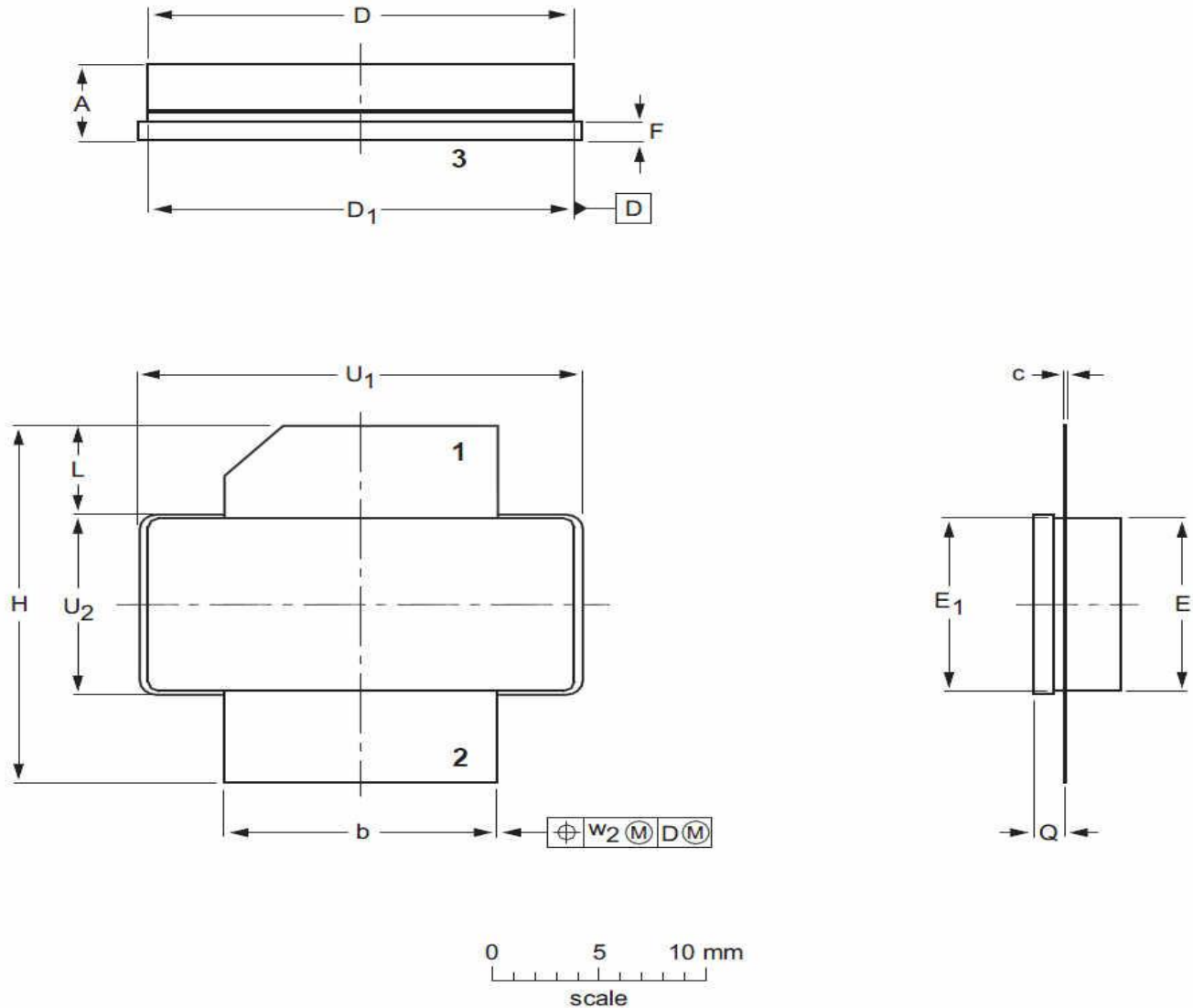


Part	Quantity	Description	Part Number	Manufacture
C1,C3,C4	3	12pF High Q Capacitor	251SHS120BSE	TEMEX
C2	1	12pF High Q Capacitor	251SHF120BSE	TEMEX
C5	1	10uF MLCC	GRM32EC72A106ME05	Murata
R1	1	10 Ω Power Resistor	ESR03EZPF100	ROHM
T1	1	300W GaN Transistor	STBV27W300BY2	Innegration



Package Outline

Earless flanged ceramic package; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	Q	U ₁	U ₂	W ₂
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2025/10/13	V1.0	Preliminary Datasheet Creation

Application data based on: LWH-25-40

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