



10W,50V Plastic RF LDMOS Transistor

ITGV22010P3

Description

The ITGV22010P3 is a 10-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies up to 2.2GHz, in 6*5mm DFN plastic package, supporting surface mounted on PCB through high density grounding vias



- Typical **multiple broadband** Class AB RF Performance

(On different Innegration fixture with device soldered) $V_{ds}=50V$ $I_{dq}=35mA$

Freq (MHz)	Pulse CW Signal ⁽¹⁾			$P_{avg}=30dBm$ WCDMA Signal ⁽²⁾		
	Gain P1dB (dB)	P3dB (W)	Eff@P3dB (%)	Gp (dB)	Eff(%)	ACPR _{5M} (dBc)
1800-2200	17	11	48	18	16	-40
1200-1600	18	11	50	19	17	-41
700-960	21	11	55	20	20	-40

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- P L, S band power amplifier
- All 4G/5G cellular application within 0.5 to 2.2GHz

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c=85^{\circ}C$, $T_j=200^{\circ}C$, DC test	$R_{\theta JC}$	6.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

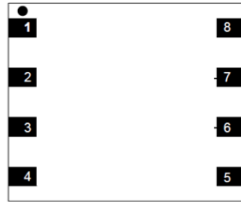


Drain-Source Voltage $V_{GS}=0, I_{DS}=100\mu A$	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 90V, V_{GS} = 0V$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 11V, V_{DS} = 0V$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 50V, I_D = 600\mu A$)	$V_{GS(th)}$	—	2	—	V
Gate Quiescent Voltage ($V_{DD} = 50V, I_D = 25mA$, Measured in Functional Test)	$V_{GS(Q)}$	—	3.4	—	V

Load Mismatch (In Innegration Test Fixture, 50 ohm system): $V_{DD} = 50Vdc, I_{DQ} = 25mA, f = 2200MHz$

VSWR 10:1 at 10W pulse CW Output Power	No Device Degradation
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Pin Configuration and Description(Top view)



Pin No.	Symbol	Description
1,2,3,4	RF IN/VGS	Gate Bias/RF Input
5,6, 7,8	RF OUT /VDS	RF Output, Drain Bias
Backside metal	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

700-960MHz application board

Reference Circuit of Test Fixture Assembly Diagram

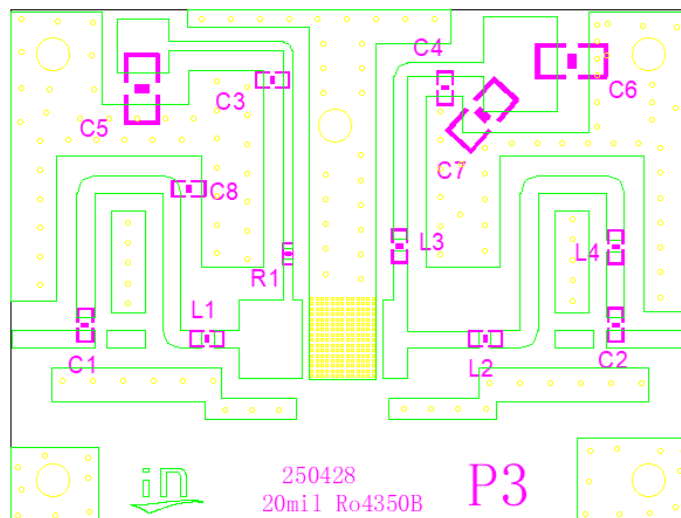


Figure 2. Test Circuit Component Layout



Table 5. Test Circuit Component Designations and Values

Reference	Quantity	Value	Footprint
C1,C2,C3,C4	4	100pF High Q Capacitor	251SHS101BSE
C8	1	1.6pF High Q Capacitor	251SHS1R6BSE
L1	1	4.7nH Inductance	/
L2	1	10nH Inductance	/
L3	1	12nH Inductance	/
L4	1	1.5nH Inductance	/
C5,C6,C7	3	10uF MLCC	GRM32EC72A106ME05
R1	1	10 Ω Power Resistor	ESR03EZPF100

TYPICAL CHARACTERISTICS

Figure 2. Power Gain and Drain Efficiency as function of Power Output

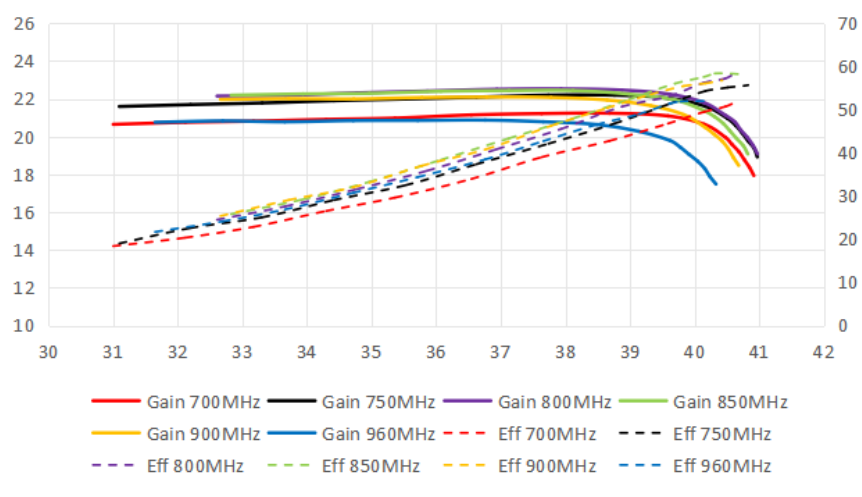
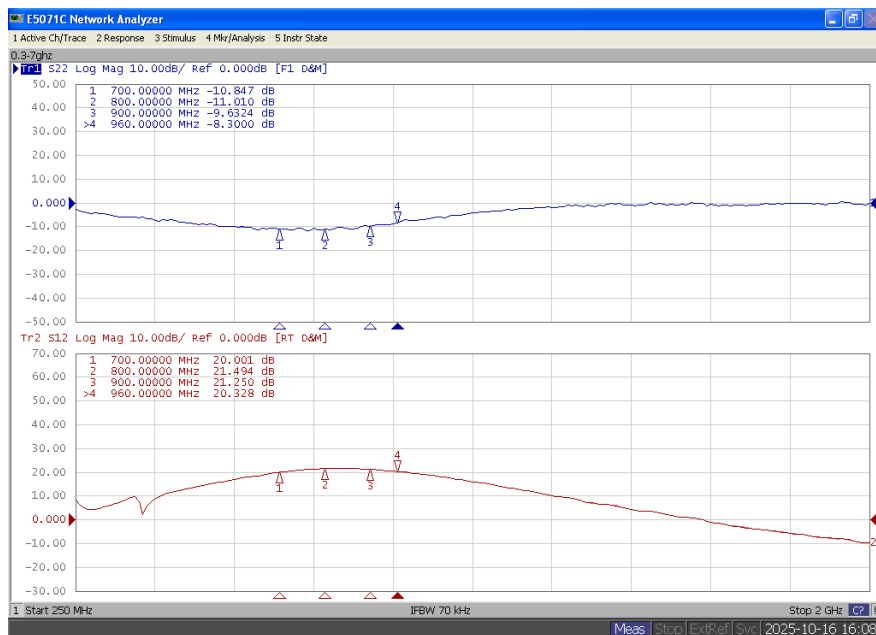


Figure 3. Network analyzer output S11/S21



1.2-1.6GHz application board

Reference Circuit of Test Fixture Assembly Diagram

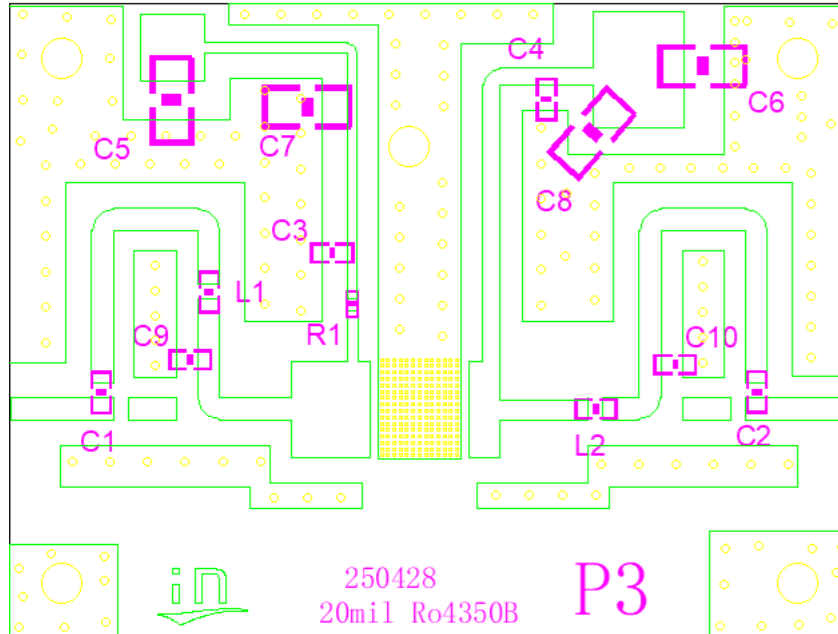


Figure 2. Test Circuit Component Layout

Table 6. Test Circuit Component Designations and Values

Reference	Quantity	Value	Footprint
C1	1	3.9pF High Q Capacitor	251SHS3R9BSE
C2,C3	2	56pF High Q Capacitor	251SHS560BSE
C4	1	100pF High Q Capacitor	251SHS101BSE
C9	1	4.7pF High Q Capacitor	251SHS4R7BSE
C10	1	0.8pF High Q Capacitor	251SHS0R8BSE
L1	1	2.2nH Inductance	/
L2	1	3.3nH Inductance	/
R1	1	10 Ω Power Resistor	ESR03EZPF100
C5,C6,C7,C8	4	10uF MLCC	GRM32EC72A106ME05

TYPICAL CHARACTERISTICS

Figure 4. Power Gain and Drain Efficiency as function of Power Output at $I_{dq}=30\text{mA}$

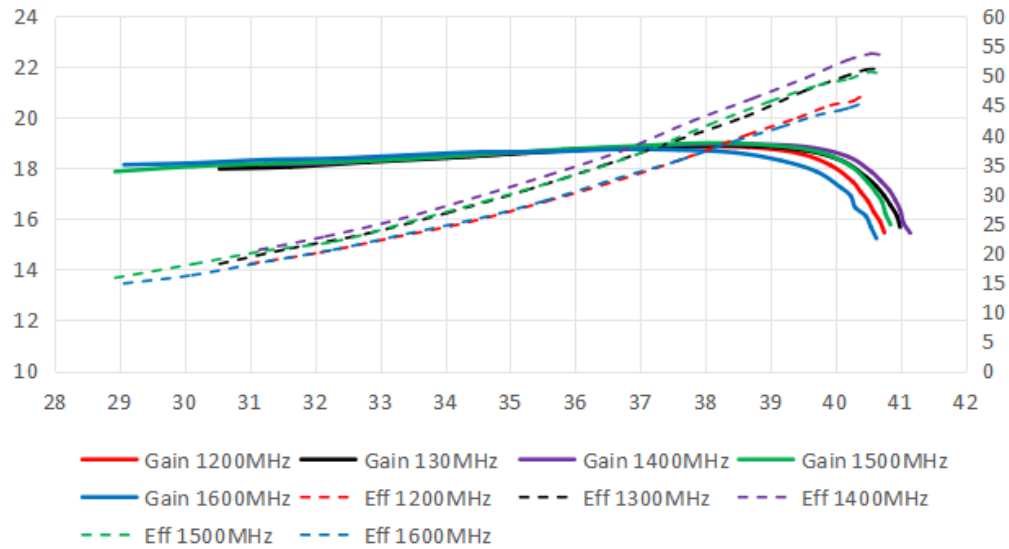
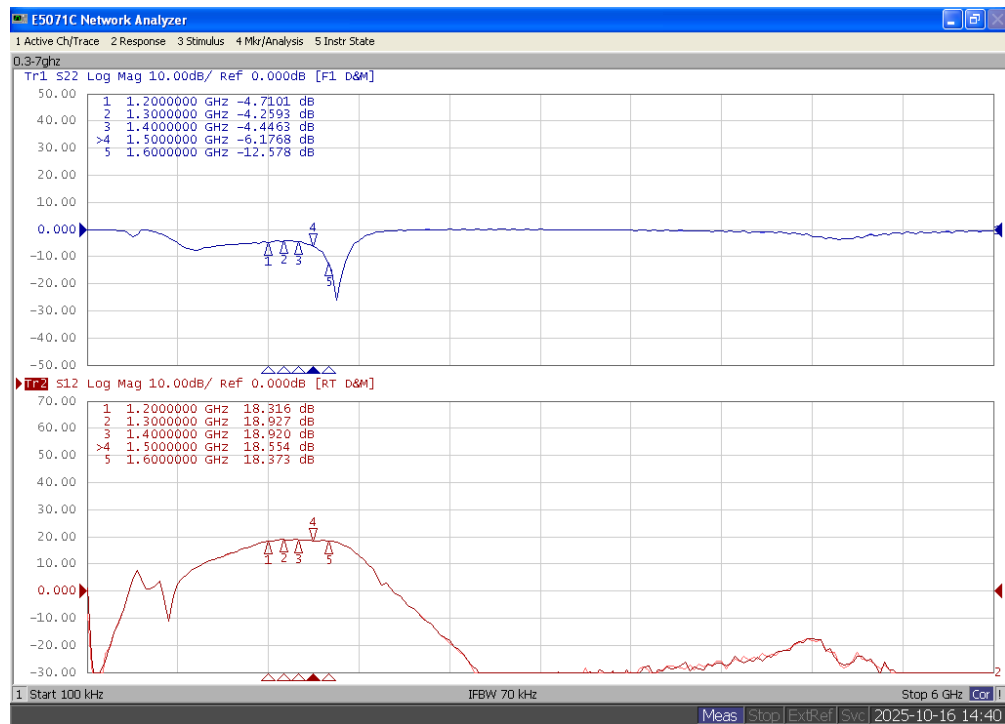


Figure 5. Network analyzer output S11/S21



1800-2200MHz application board

Reference Circuit of Test Fixture Assembly Diagram

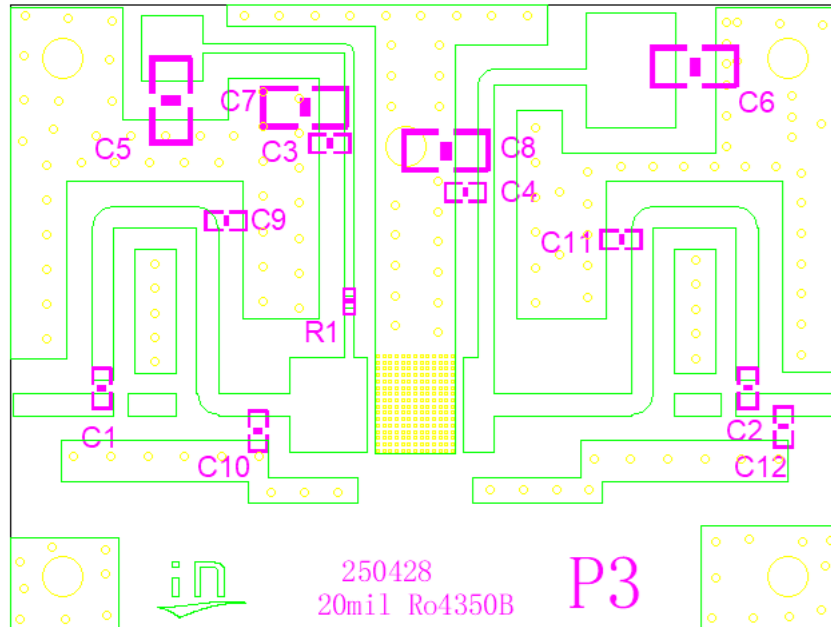


Figure 6. Test Circuit Component Layout

Table 7. Test Circuit Component Designations and Values

Reference	Quantity	Value	Footprint
C1,C2,C3,C4	4	20pF High Q Capacitor	251SHS200BSE
C9	1	3.9pF High Q Capacitor	251SHS3R9BSE
C10,C11	2	1.5pF High Q Capacitor	251SHS1R5BSE
C12	1	0.5pF High Q Capacitor	251SHS0R5BSE
R1	1	10 Ω Power Resistor	ESR03EZPF100
C5,C6,C7,C8	4	10uF MLCC	GRM32EC72A106ME05



TYPICAL CHARACTERISTICS

Figure 7. Power Gain and Drain Efficiency as function of Power Output at $I_{DQ}=35\text{mA}$

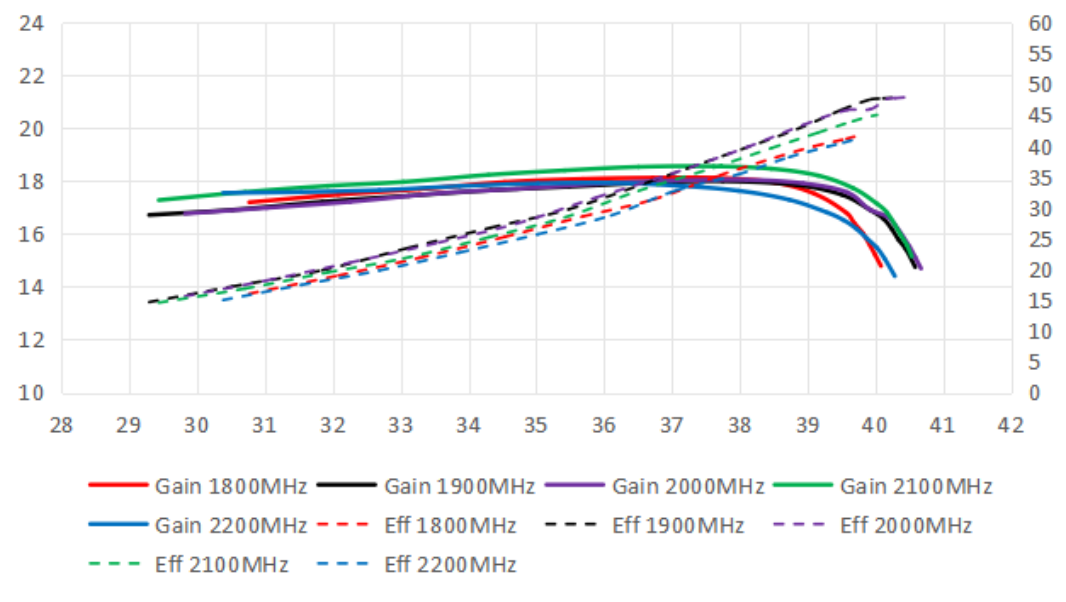
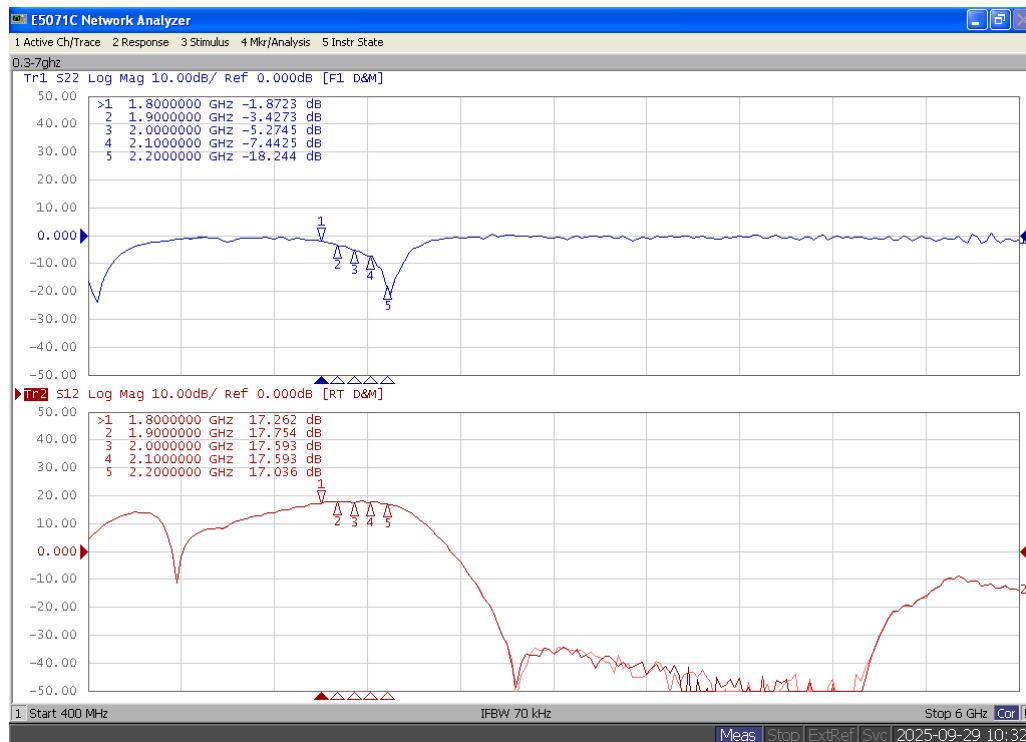


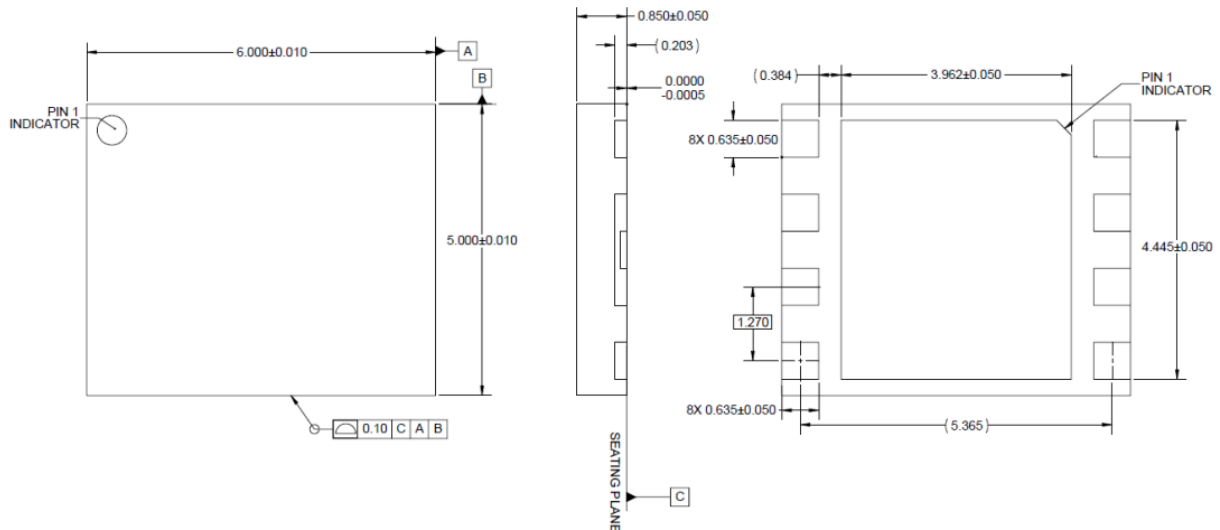
Figure 8. Network analyzer output S11/S21





Package

6*5 DFN Package



Notes:

1. All dimensions are in mm. Otherwise noted, the tolerance is ± 0.1 mm.
2. Package leads are gold plated.
3. Part is mold encapsulated.

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2025/10/17	Rev 1.0	Preliminary Datasheet

Application data based on HZH-25-10/11/12

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